GOVERNMENT POLYTECHNIC BHUBANESWAR

LECTURE NOTE

ON

Microprocessor and Microcontroller – TH-3

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Unit-1:Microprocessor(ArchitectureandProgramming-8085-8-bit).

:IntroductiontoMicroprocessorandMicrocomputer&distinguishbetween them.

Microprocessor:isacomputerprocessorwhichincorporatesthefunctionsofacomputer'scentralprocessingunit (CPU) on a single integrated circuit (IC) at most a few integrated circuits. The microprocessor is a multipurpose, clockdriven,registerbased,digital-integratedcircuitwhichacceptsbinarydataasinput,processesitaccordingto instructions stored in its memory, and provides results as output. Microprocessors contain both combinational logic and sequential digital logic. Microprocessors operate on numbers and symbols represented in the binary numeral system.

Any microprocessor based system having limited number of resources are called **microcomputers**. The main difference between microprocessor & microcomputer is that the microprocessor is a computer processor contained on an integral circuit chipand **microcomputer** is a small, relatively inexpensive computer.

: Concept of Address Bus,Data Bus, Control bus& System Bus.

Busisagroupofconductingwiresthroughwhichsignalsarepasses.

Abuswhichisusedtoprovidethecommunicationbetweenthemajorcomponentsofacomputeriscalled as**SystemBus**.Asystembusisasinglebusthatconnectsthemajorcomponentsofacomputersystem,combining thefunctionsofadatabustocarryinformation.The**ControlBus**isusedtocarrynecessarycontrolsignalsbetween the CPU and memory and I/O devices. A**control bus**is a computer **bus**that is used by the CPU to communicate with devices that are contained within the computer.

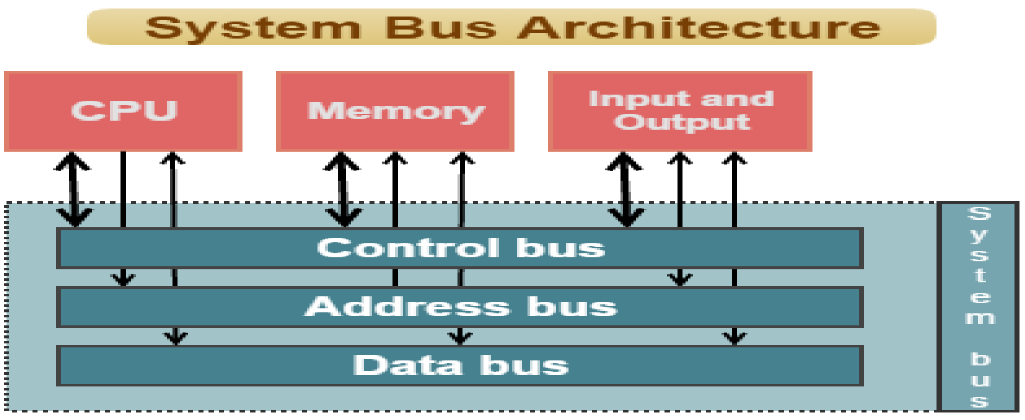
Thereare3typesofBusesareused.

- **AddressBus**
- **DataBus**
- **ControlBus**

The **Address bus** carries the address of a memory location or I/O device that the CPU wants to access. It is a unidirectional bus. The width of the address bus is decided by the designed memory addressing capability of the CPU.For exampleIntel 8085has 16-bitaddress bus whichgives 2tothe power 16=64K bytememory **addressing capability.**

The width of **Data bus** is same as the word length of the CPU. **Data bus** has 8-bit length and it is used to transfer databetweentheCPU,memoryandI/Odevices.Bothaddressbus&**ControlBus**areunidirectionalwhereasdata bus is bi-directional.

:GeneralBusstructureBlock diagram.



:BasicArchitectureof8085(8 bit) Microprocessor.

Intel 8085is a 8-bit, NMOS Microprocessor that can deal with the memory of 64K Byte. This microprocessor consists of 40-pins as well as works with +5V power supply. This processor can be work at a 3MHz of maximum frequency. This processor is available in three versions such as 8085 AH, 8085 AH1, and 8085 AH2 which are designedwithHMOStechnology.Thehighlydevelopedversionsuse20%ofthepowersupply.TheCLKfrequencies of the versions of this processor are 8085 A- 3 MHz, 8085AH-3 MHz, 8085 AH2-5 MHz, and 8085 AH1

ALU: Thearithmeticandlogicunit,ALUperformsthefollowingarithmeticandlogicaloperation.

a. Addition.
b. Subtraction.
c. LogicalAND
d. LogicalOR
e. LogicalExclusiveOR
f. Complement
g. Increment
h. Decrementetc.

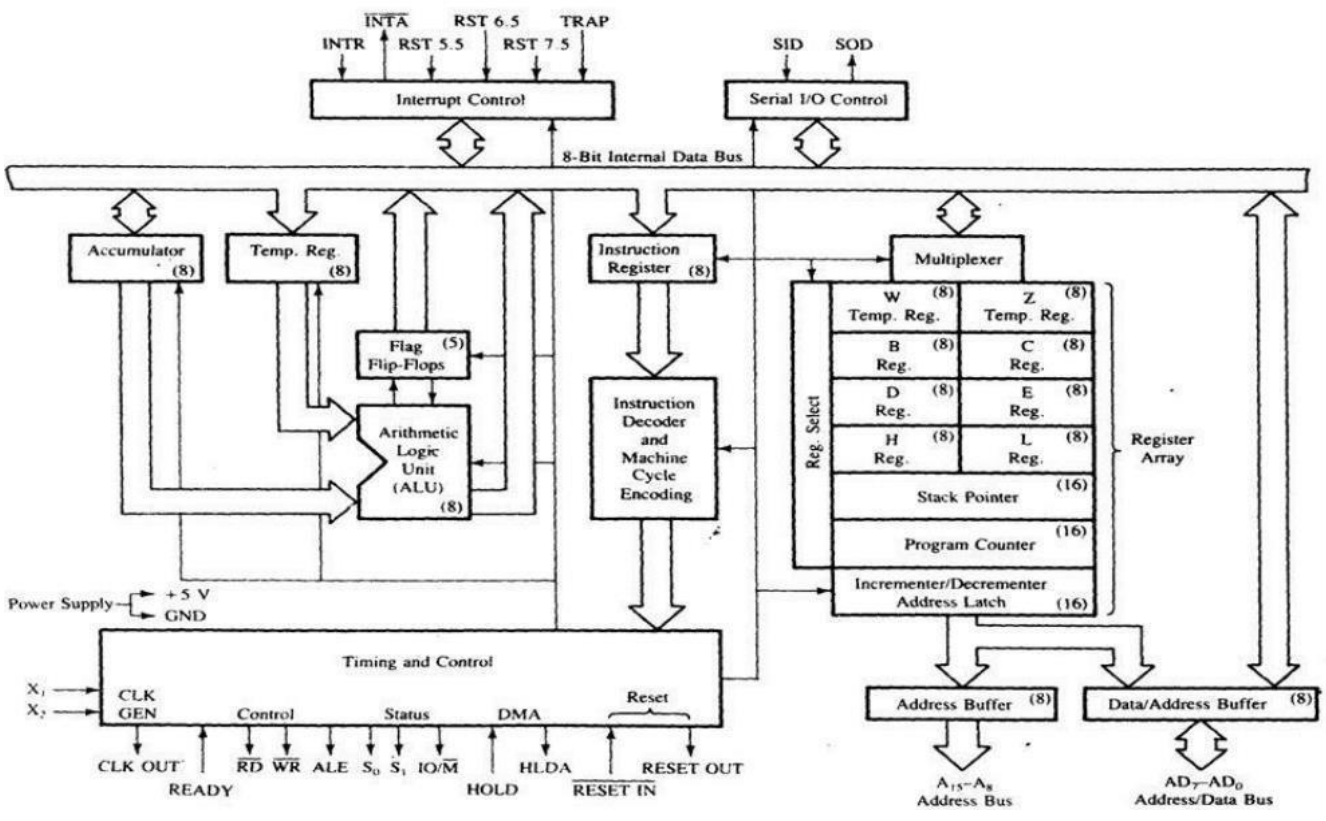
Timingand ControlUnit:

TheTiming&ControlUnitisasectionoftheCPU

Registers: Registers are used by the microprocessor for temporary storage and manipulation of data and instructions. Data remain in the registers till they are sent to the memory or I/O devices. In a large computer the number of registers is more andhence the programrequires less transfer of datato/fromthe memory.In asmallcomputerthenumberofregistersissmallduetolimitedsizeofthechip.Intel8085microprocessorhas the following registers.

- One8-bitaccumulator(ACC)i.eregisterA
- Six8-bitGeneralPurposeRegisters.TheseareB,C,D,E,HandL
- One16-bitStackPointer,SP
- One16-bitProgramCounter,PC
- InstructionRegister
- TemporaryRegister

The 8085 Architecture



ACCUMULATOR (ACC): The accumulator is an 8-bit register associated with the ALU. The register **'A'** in the 8085 is an Accumulator. It is used to hold one of the operands of an arithmetic or logical operation. It serves as one input to the ALU. The other operand for an arithmetic or logical operation may be stored either in the memoryorinoneofthe**GeneralPurposeRegisters(GPR)**.Thefinalresultofanarithmeticorlogicaloperations placed in the Accumulator. Such instructions do not require any other register or memory location because there is noother operand.There is one typicalinstructionDAD rp,for 16-bitadditionfor whichone of the 16- bit operands is kept in H-L pair and the other in the B-C or D-E pair . The result is placed in the H-L pair.

GeneralPurpose Registers (GPR):The 8085 microprocessor contains six 8-bit general purposeregisters.They are: B,C,D,E,HandHandLregister.Tohold16bitdataacombinationof two 8-bitregisters canbe employed. The combination of two 8-bit registers is known as a register pair. The valid register pairs in the 8085 are: B- C,D-EandH-L.Theprogrammercannotfromaregisterpairbyselectinganytworegistersofhischoice.TheH- L pair is used to act as memory pointer and for thispurpose it holds the 16-bit address of a memory location. The general purpose registers and the accumulator are accessible to programmer. He can store data in these registers during writing his program.

SpecialPurposeRegister (SPR):

- **Program Counter (PC)**: It is a 16-bit special purpose register. It is used to hold the memory address of the next instruction to be executed. It keeps the track of memory addresses of the instructions in a programwhiletheyarebeingtheexecutionofaninstructionsothatitpointstotheaddressofthenext instruction in the program at the end of the execution of an instruction.
- **Stack Pointer (SP)**: It is a 16 bit special purpose register. The stack is a sequence of memory locations setasidebytheprogrammertostore/retrievethecontentsofAccumulator.SincestackworksonLIFO (Last-In-First-Out)principle,itsoperationisfastercomparedtonormalmemorylocations.Thecontents

of only those registers are saved, which are needed in the later part of the program. The SP holds the address of the top element of data stored in the stack.

Instruction Register: The Instruction Register holds the op-code (Operation Code) of the Instruction which is being decoded and executed.

Temporary Register: It is an 8-bit register associated with the ALU. It holds data during an arithmetic/logical operation.

Flags: The Intel 8085 microprocessor contains five flags to serve as status flags. The Flip Flops are set or reset according to the conditions which arise during arithmetic or logical operation. If a flip flop for a particular flag is set, it indicates 1, when it reset, it indicates 0.

a.Carry Flag(CS) b.ParityFlag(P)
c. AuxiliaryCarryFlag(AC) d.ZeroFlag(Z)
e.SignFlag(S)

Carry Flag (CS): After addition of two 8 bit no, if the sum is larger than 8 bit, acarry is produced and carry flag (CS) is set to 1 **or** in case of subtraction if borrow occurs then CS is set to 1, otherwise it is 0.

Parity Flag(P): It isset to 1, If the result of an arithmetic operation/ logical operation contains even no of 1s, if odd no of 1s, it is set to 0.

AuxiliaryCarryFlag(AC): Ifitholdsthe carryfrom3rd bitto4thbititissetto1,otherwiseitis 0.

ZeroFlag(Z):Z issetto1,Iftheresultofanarithmeticoperation/ logical operationis0.Iftheresultisnot Zero, it is set to 0.

SignFlag(S): TheSignflagSissetto1,iftheresultofanarithmeticoperation/logicaloperationisnegative, If the result is positive, it is set to 0.

PSW: FivebitsindicatesstatusFlagandthreeflagsindicatesundefined.Thecombinationof8 bitiscalled **ProgramStatusWord(PSW).**

Ex: 1100 101 1CB
<u>1110 1001E9</u>
11011 0100

7 6 54 3 2 1 0 Bitno

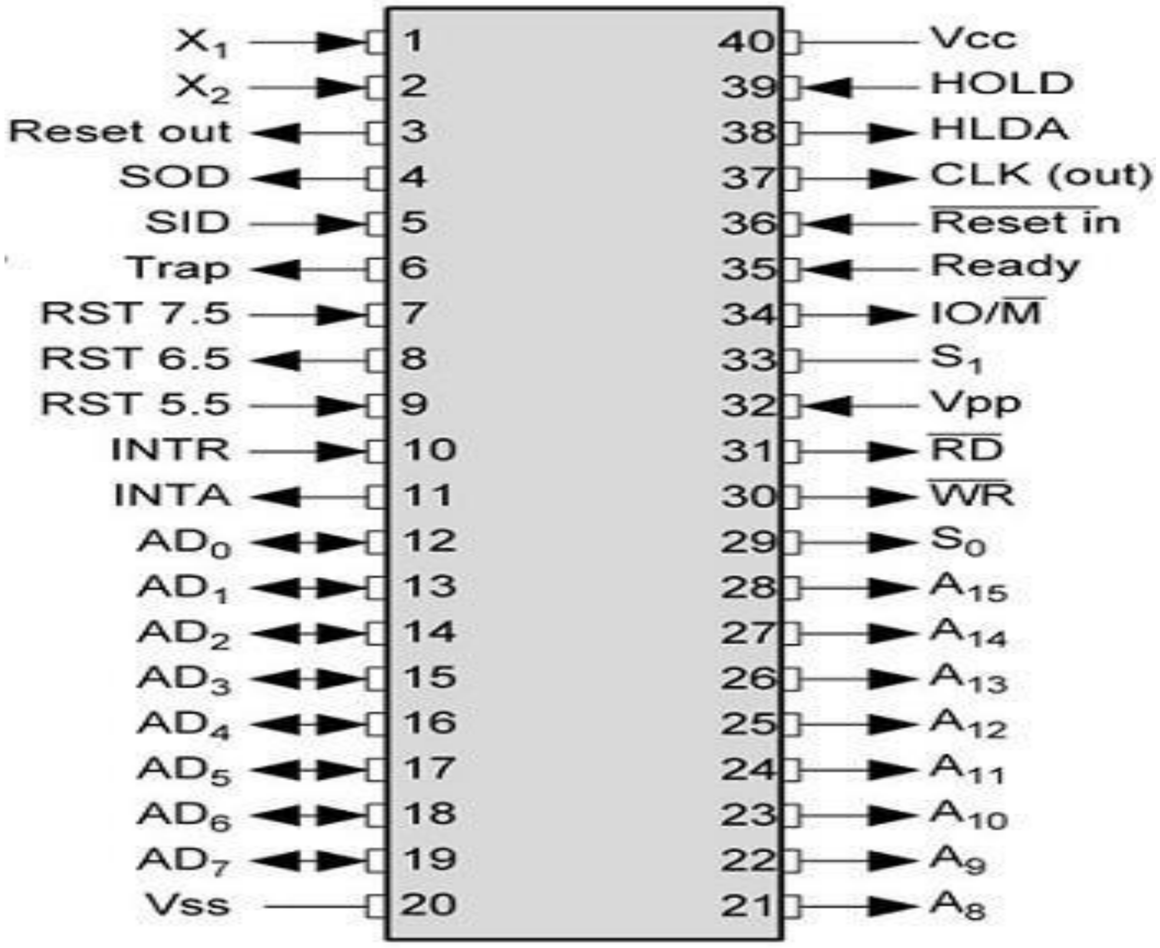
S	Z	X	AC	X	P	X	CS
1	0	1	1	0	1	0	0

1. Thereis a carryCSissetto1.
2. P is setto1,evennoof1s.
3. There is a carryfrom3rd to4thbitACissetto1.
4. Resultis Non-ZeroZis0.
5. MSBof theSumis1,Sissetto1.

:SignalDescription(Pindiagram)of8085Microprocessor.

<u>PinDiagramofIntel8085Microprocessor</u>

The 8085<u>microprocessor is an 8-bit general purpose processor</u> that can deal with the memory of 64K Byte. This microprocessorconsistsof40-pinsas wellasworkswith+5V<u>powersupply</u>.Thisprocessorcanbeworkata3MHz of maximum frequency. This processor is available in three versions such as 8085 AH, 8085 AH1, and 8085 AH2 which are designed with HMOStechnology. The highly developed versions use 20% ofthe power supply. The CLK frequencies of the versions of thisprocessor are 8085A- 3MHz, 8085AH-3MHz, 8085AH2-5MHz, and 8085AH1



AddressBus(A8-A15)(output):

Theaddressbuspinsarerangesfrom**A8toA15**andthesearemainlyapplicabletothemostconsiderablememory address bit.

AddressBusandData Bus: (Input/Output):

The address bus is a group of sixteen lines i.e A0-A15. The address bus is unidirectional. These are time multiplexedaddress/datai.etheyservedualpurpose.Theyareusedfor8bitLSBofthememoryaddressorI/O address during 1st clock cycle of a machine cycle. Again they are used for data during 2nd and 3rd clock cycle.

Address Latch Enable (ALE)(output)– It is an Address Latch Enable signal. It goes high during first T state of a machinecycleandenables thelower8-bitsoftheaddresstobelatchedeitherintothememoryorexternallatch.

- **IO/M'(output) –**Itisa statussignalwhich determines whether the address isforinput-output or memory. When it is high(1) the address on the address bus is for input-output devices. When it is low(0) the address on the address bus is for the memory.
- **SO,S1(output)–**Thesearestatussignalssentbythemicroprocessor.Theydistinguishthevarioustypesof operations such as halt, reading, instruction fetching or writing.

S1	S0	Operations
0	0	HALT
0	1	WRITE
1	0	READ
1	1	FETCH

Power SupplyandClockFrequency:

- **Vcc–**+5vpower supply
- **Vss–**GroundReference
- **XI,X2(input)–**Thesearetheterminalstobeconnectedtoanexternalcrystaloscillatorwhichdrivesan internalcircuitryofthemicroprocessortoproducea suitableclockforthe operationofmicroprocessor. The

frequencyisinternallydividedbytwo,therefore,tooperateasystemat3MHZthecrystalshouldhave frequency of 6MHZ.

- **CLK(OUT)–**Thissignalcanbeusedasthesystemclockforotherdevices. Itsfrequencyissameatwhich processor operates.

  READY(input)–Itisusedbythemicroprocessortosensewhetheraperipheralisreadytotransferdataor not. If READY is high the peripheral is ready. If it is low the microprocessor waits till it goes high.

  RD'(output) –ItisasignaltocontrolREAD operationWhenitgoeslowtheselectedmemoryorI/Odevice is read.

  WR'(output) –ItisasignaltocontrolWRITEoperation.Whenitgoeslowthedataonthedatabusis written in to selected memory or I/O location.

The8085hasfiveinterruptsignalsthatcanbeusedtointerruptaprogram execution.

(i) TRAP
(ii) RST 7.5
(iii) RST 6.5
(iv) RST 5.5
(v) INTR

TRAP

These are interrupts. The microprocessor acknowledges Interrupt Request by INTA' signal. In addition to Interrupts,thereare threeexternallyinitiatedsignalsnamelyRESET,HOLDandREADY.TorespondtoHOLD request, it has one signal called HLDA.

- **INTR(input)–** Itisaninterruptrequestsignal.
- **INTA'(output)–**ItisaninterruptacknowledgmentsentbythemicroprocessorafterINTRisreceived.
- **RESET IN'(input)–**Whenthesignalonthispinislow(0),theprogram-counterissettozero,thebusesare tristated and the microprocessor unit is reset.
- **RESET OUT (output) –**ThissignalindicatesthattheMPUisbeing reset.Thesignalcanbeusedtoreset other devices.

- **HOLD(input)–**Itindicatesthatanotherdeviceisrequestingtheuseoftheaddressanddatabus.Having received HOLD request the microprocessor relinquishes the use of the buses as soon as the current machine cycle is completed.Internal processing may continue. After the removal of the HOLDsignal the processor regains the bus.
- **HLDA(output) –**Itisasignalwhichindicatesthattheholdrequesthasbeenreceivedaftertheremovalofa HOLD request, the HLDA goes low.

Serialtransmissionin8085isimplementedbythetwosignals,

- **SID(input)–**SIDisadatalineforserialinput.Thedataonthislineisloadedinto7thbitoftheaccumulator when RIM instruction is executed.
- **SOD(output) –**SODisadatalineforserialoutput. The7thbitoftheaccumulatorisoutputonSOD line when SIM instruction is executed.

:RegisterOrganizations,DistinguishbetweenSPR& GPR,Timing&Control Module.

A**register**is a temporary storage area built into a CPU. Some **registers**are used internally and cannot be accessedoutsidetheprocessor,whileothersareuser-accessible.MostmodernCPUarchitecturesincludeboth types of **registers.** These**registers**are used to storeor copy temporary data, by using instructions, during the execution of the program.

TherearetwotypesofregisterinIntel8085Microprocessor.

a. **GeneralPurposeRegisters(GPR)**
b. **SpecialPurposeRegister(SPR)**

Register organization is the arrangement of the **registers**in the processor. The processor designers decide the **organization** of the **registers** in a processor.

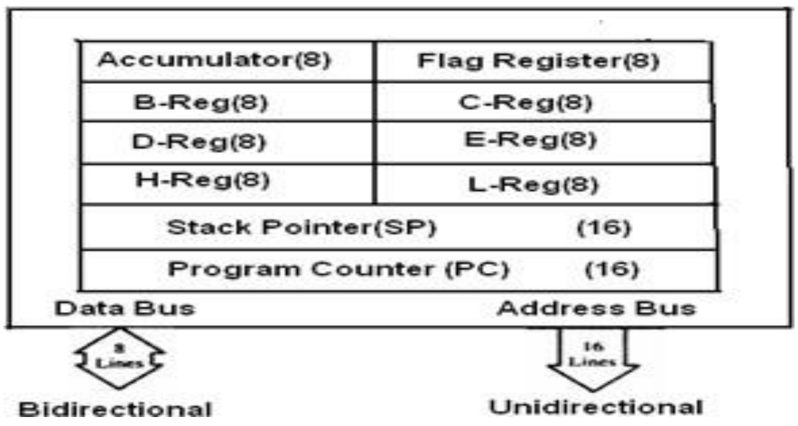


Fig.Register organization

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1.7.Stack,Stackpointer&stacktop:

Stack: During the execution of a programme sometimes it becomes necessary to save the contents of certain registersbecausetheregistersarerequiredforsomeother operationinlaterstage.Thesecontentsaremovedto memorylocationsby **PUSH**operation.After completingtheseoperationsthosecontentswhich weresavedinthe memoryaretransferredbacktotheregistersby**POP**operation.Thesetofmemorylocationskeptforthispurpose is called **Stack.**

The last memory location of the stack is called **Stack Top.** The**Stack**Pointer register will hold the address of the top location of the **stack**.

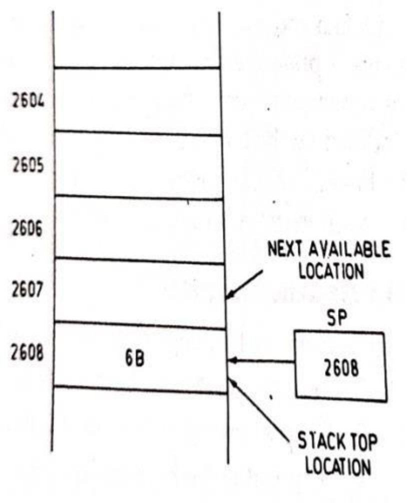


Fig. 5.1. Stack and stacktop location.

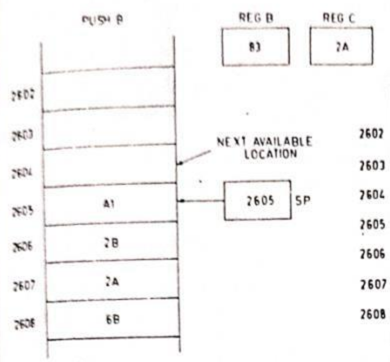


Fig. 5.2 (a). Stack before PUSH operation.

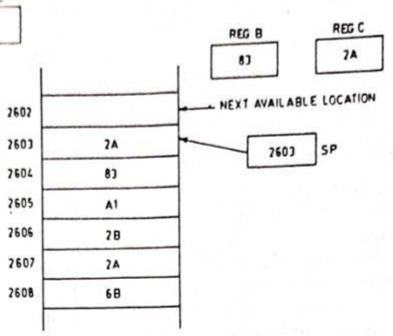


Fig. 5.2 (b). Stack after PUSH operation.

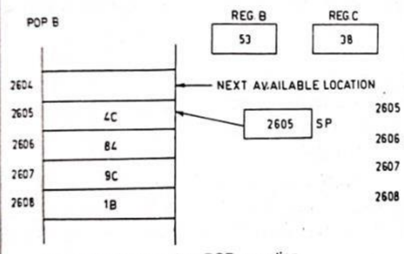


Fig. 5.3 (a). Stack before POP operation.

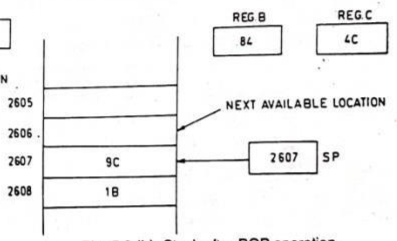
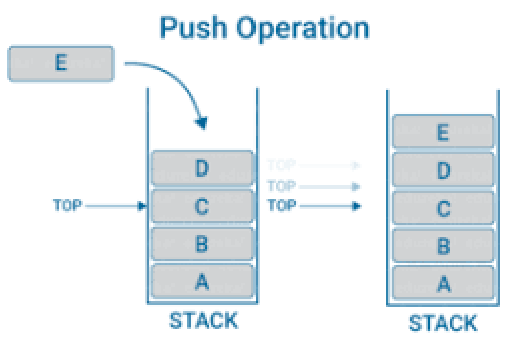
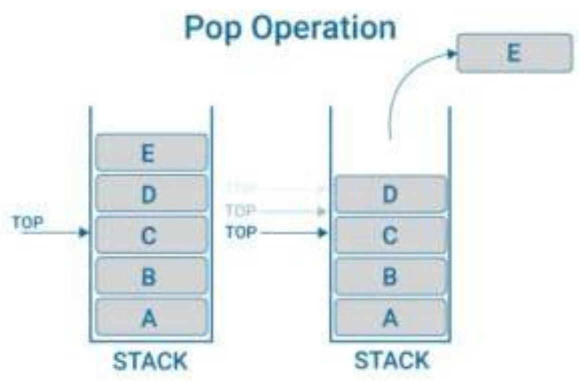


Fig. 5.3 (b). Stack after POP operation.

StackPointer(SP): Itis a16bitspecialpurpose register.The stack is asequence of memory locations setaside by the programmer to store / retrieve the contents of Accumulator. Since stack works on **LIFO (Last-In-First-Out)** principle, its operation is faster compared to normal memory locations. The contents of only those registers are saved, which are needed in the later part of the program. The SP holds the address of the top element of data stored in the stack.





1.8:Interrupts:-8085Interrupts,MaskingofInterrupt(SIM,RIM).

<u>Interruptsin8085</u>

Interrupts are the signals generated by the external devices to request the microprocessor to perform a task.There are 5 interrupt signals, i.e. **TRAP, RST 7.5, RST 6.5, RST 5.5, and INTR.**

Interruptareclassifiedinto followinggroupsbasedontheirparameter−

- **Vectorinterrupt**−Inthistypeofinterrupt,theinterruptaddressisknowntotheprocessor. **For example:** RST7.5, RST6.5, RST5.5, TRAP.
- **Non-Vector interrupt** − In this type of interrupt, the interrupt address is not known to the processor so, theinterruptaddressneedstobesentexternallybythedevicetoperforminterrupts. **Forexample:**INTR.
- **Maskable interrupt** − In this type of interrupt, we can disable the interrupt by writing some instructions into the program. **For example:** RST7.5, RST6.5, RST5.5.

- **Non-Maskableinterrupt**−Inthistypeofinterrupt,wecannotdisabletheinterruptbywritingsome instructionsintotheprogram.**Forexample:**TRAP.
- **Softwareinterrupt**−Inthistypeofinterrupt,theprogrammerhastoaddtheinstructionsintotheprogram toexecutetheinterrupt.Thereare8softwareinterruptsin8085,i.e.RST0,RST1,RST2,RST3,RST4,RST5, RST6, and RST7.
- **Hardware interrupt** − There are 5 interrupt pins in 8085 used as hardware interrupts, i.e. TRAP, RST7.5, RST6.5, RST5.5, INTA.

Note−INTA is not an interrupt, it is used by the microprocessor for sending acknowledgement. TRAP has the highest priority, then RST7.5 and so on.

InterruptServiceRoutine (ISR)
Asmallprogramoraroutinethatwhenexecuted,servicesthecorrespondinginterruptingsourceiscalledan ISR.

The8085hasfiveinterruptsignalsthatcanbeusedtointerruptaprogramexecution.
(i) TRAP
(ii) RST7.5
(iii) RST6.5
(iv) RST5.5
(v) INTR
TRAP
TRAPisanon-maskableinterrupt,havingthehighestpriorityamongallinterrupts.Bydefault,itisenableduntilit getsacknowledged.Incaseoffailure,itexecutesas**ISR**andsendsthedatatobackupmemory.Themicroprocessor acknowledges Interrupt Request by INTA' signal. In addition to Interrupts, there are three externally initiated signals namely RESET, HOLD and READY. To respond to HOLD request, it has one signal called HLDA.

- **INTR–** Itisaninterruptrequestsignal.
- **INTA'–**Itisaninterruptacknowledgmentsentbythemicroprocessorafter INTRisreceived.

RST7.5
Itisamaskableinterrupt,havingthesecondhighestpriorityamongallinterrupts.Whenthisinterruptisexecuted, the processor saves the content of the PC register into the stack and branches to 003CH address.

RST6.5
It is a maskable interrupt, having the third highest priority among all interrupts. When this interrupt is executed, the processor saves the content of the PC register into the stack and branches to 0034H address.
RST5.5
Itisamaskableinterrupt.Whenthisinterruptisexecuted,theprocessorsavesthecontent ofthePCregisterinto the stack and branches to 002CH address.
INTR
It is a maskable interrupt, having the lowest priority among all interrupts. It can be disabled by resetting the microprocessor.

SIM:SetInterruptMask
It is a 1 byte instruction and it is a multi-purpose instruction. The main use of SIM instruction are-Masking/unmasking of RST 7.5, RST6.5 and RST 5.5. It is used for Serial output of Data (SOD).

RIM:Read Interrupt Mask
Itisused
Tocheckwhether RSTaremaskedornot.
Tocheckwhetherinterruptsareenableornot. To
perform Serial input data (SID).

:Addressing data& Differentiatebetweenone-byte,two-byte&three-byteinstructionswith examples.

A Digital Computer understands instructions written in binary codes (machine codes). The machine codes of all instructions are not of the same length. According to the word size Intel 8085 instructions are classified into the following three types.

1. 1-byte instruction.
2. 2- byteinstruction.
3. 3-byte instruction.

<u>Examples of 1-byte instruction.</u>

MOVA,B	machinecode=78
ADDB	machinecode=80
RAL	machinecode=17
HLT	machinecode=76

<u>Examplesof2-byte instruction.</u>

A2byteInstructionisstoredintwoconsecutivememory location.

MVIB,05 machinecode=06,05

The1st byte06isthemachinecodeforMVIBand2nd byte05isthedatawhichistobemovedtoregister B.

IN01 machinecode= DB,01

DBisthemachinecodefortheinstructionINand01 istheaddressofaportBforinterfacing.

<u>Examplesof3-byte instruction.</u>

LXIH,2400H	machinecode=21,00,24
LDA2500H	machinecode=3A,00,25

:Addressingmodesininstructionswithsuitableexamples.

<u>AddressingModesofIntel8085Microprocessor</u>

The way of specifying data to be operated by an instruction is known as **addressing modes**.Each instruction requires certain data on which it has to operate. There are various types of techniques to specify data for instructions. These techniques are called **addressing modes.**

Thereare5typesofaddressing modesareused

1. DirectAddressing Mode.
2. RegisterAddressingMode.
3. RegisterIndirectAddressingMode.
4. ImmediateAddressing Mode.
5. ImplicitAddressing Mode.

1. **DirectAddressingMode:**Inthismodeofaddressingtheaddressoftheoperand(data)isgiveninthe instruction itself.
    1. **STA2400H**
       (32,00,24)Storethecontentoftheaccumulatorinthememorylocation2400H.
    2. **IN02**
       (DB,02)ReaddatafromtheportC.
2. **RegisterAddressingMode:**InRegisterAddressingModetheoperandisoneoftheGeneralPurpose Register.The opcodespecifiesthe address ofthe registerinadditiontotheoperationtobe performed.
    1. **MOV A,B**
       (78)MovethecontentofregisterBtoregisterA.

2. **ADDB**
(80)AddthecontentofregisterBtothecontentofregisterA.

3. **Register Indirect Addressing Mode:** In this mode of addressing the address of the operand is specifiedby a register pair.
   1. **LXIH,2100H**
      MOV A,M
      HLT
   (MOVA,MistheexampleofregisterindirectAddressingMode)
   2. **LXIH,2500H**
      ADD M
      HLT
      (ADDMistheexampleofregisterindirectAddressing Mode)
4. **ImmediateAddressingMode:**InimmediateAddressingModetheoperandisspecifiedwithintheinstruction itself.
   1. **MVIA,05.**
   2. **ADI06**
   (ExamplesofImmediateAddressingMode)
5. **ImplicitAddressingMode:**Therearesomeinstructionswhich operateonthecontentoftheaccumulator. Such instructions do not require the address of the operand. **Ex-CMA, RAL, RAR.**

:InstructionSetof8085(DataTransfer,Arithmetic,Logical,Branching,Stack&I/O,Machine Control).

In**microprocessor**, the**instruction set** is the collection of the **instructions**that the**microprocessor**is designed to execute. The programmer writes a program in assembly language using these **instructions**. An**instruction** is a binarypatterndesignedinsidea **microprocessor** toperformaspecificfunction.Theentiregroup of **instructions** that a **microprocessor** supports is called **Instruction Set**.**8085** has 246 **instructions**.
These instructions are of Intel Corporation. They cannot be used by other microprocessor manufacturers. These instructions are classified into the following Groups.

a. **DataTransferGroup.**
b. **Arithmetic Group.**
c. **Logical Group.**
d. **BranchControl Group.**
e. **I/Oand MachineControlGroup.**

DataTransferGroup:
Instructionswhichareused totransferdatafromoneregistertoanotherregister,frommemorytoregisteror register to memory comes under this group.

MOVr1,r2(Movedata,Movethecontentsofoneregistertoanother)
MOVr,M(Movethecontentsofmemorytoregister)
MOVM,r(Movethecontentsofregistertomemory) **MVI**
r, data (Move Immediate data to register)
MVIM,data(MoveImmediatedatatomemory **LXI**
rp, data16 (Load register pair immediate) **LDA**
addr (Load Accumulator Direct)
STAaddr(StoreAccumulatorDirect)
LHLD addr (Load H-L pair direct)
SHLD addr (Store H-L pair direct)
LDAXrp(Loadaccumulatorindirect)
STAXrp(Storeaccumulatorindirect)
XCHG(ExchangethecontentofH-LpairtoD-Epair)

Arithmetic Group:

Theinstructionsinthisgroupperformarithmeticoperations.

ADDr(Addregister to accumulator)
ADDM(AddMemorytoaccumulator)
ADC r(Add register with carry to accumulator)
ADCM(AddMemorywithcarrytoaccumulator)
ADI data(Add immediate data to accumulator)
ACIdata(Addwithcarryimmediatedatatoaccumulator)
DADrp(AddregisterpairtoH-L pair))
SUBr(Subtractregisterfromaccumulator)
SUBM(SubtractMemoryfromaccumulator)
SBB r(Subtract register from accumulator with borrow)
SBBM(Subtractmemoryfromaccumulatorwithborrow) **SUI data**(Subtract immediate data from accumulator)
SBIdata(Subtractimmediatedatafromaccumulatorwithborrow)
INR r(Increment register content)
INR M(Increment memory content)
DCR r(Decrement register content)
DCRM(Decrementmemorycontent)
INX rp(Increment register pair)
DCXrp(Decrementregisterpair)
DAA(DecimalAdjustAccumulator)

Logical Group:
Theinstructionsinthisgroupperformlogicaloperations.

ANAr(AND registerwithaccumulator)
ANAM(ANDmemory withaccumulator)
ANIdata (AND immediatedatawithaccumulator)
ORAr(ORregisterwith accumulator)
ORAM (ORmemorywith accumulator)
ORIdata(ORimmediatedatawithaccumulator)
XRA r (Exclusive OR register with accumulator)
XRAM(ExclusiveORmemorywithaccumulator)
XRIdata(ExclusiveOR immediatedatawithaccumulator)
CMA(Complementtheaccumulator)
CMC(Complement the carry status)
STC(Set carry status)
CMPr(Compareregisterwithaccumulator)
CMPM(Comparememorywithaccumulator)
CPIdata(Compareimmediatedatawithaccumulator)
RLC(Rotateaccumulatorleft)
RRC(Rotateaccumulatorright)
RAL(Rotateaccumulatorleftthroughcarry)
RAR(Rotateaccumulatorrightthroughcarry)

BranchGroup:
Thisgroupincludestheinstructionsforconditionalandunconditionaljump,subroutinecallandreturnand restart. Therearetwotypesofbranchinstructions
1. Conditionally
2. Unconditionally

Theconditionalbranchinstructionstransfertheprogramtothespecifiedlabelwhencertainconditionissatisfied. The unconditional branch instructions transfer the program to the specified label unconditionally.

JMPaddr(label)(Unconditionaljump.totheinstructionspecifiedbythe address)
JZaddr(label)(Jumpiftheresultiszero)
JNZaddr(label)(Jumpifthe resultis notzero)
JC addr (label)(Jump if there is a carry)**JNC**
addr (label)(Jump if there is no carry) **JP**
addr (label)(Jump if the result is plus)
JMaddr(label)(Jumpiftheresultisminus) **JPE**
addr (label)(Jump if even parity)
JPOaddr(label)(Jumpif odd parity)
CALLaddr(label)(Unconditionalcall,callsubroutineidentifiedbythe address)
RET.(Returnfromsubroutine)
RSTn(Restart)
PCHL(JumptoaddressspecifiedbyH-Lpair)

Stack,I/OandMachineControlGroup:
Thisgroupincludestheinstructionsforinput/outputports,stackandmachinecontrol.

IN port-address(Input to accumulator from I/O port)
OUTport-address(OutputfromaccumulatortoI/Oport)
PUSH rp(Push the content of register pair to stack)**PUSH**
PSW(PUSH Processor Status Word)
POPrp(Popthecontentofregisterpair,whichwassaved,fromthestack)
POPPSW(POPProcessorStatusWord)
HLT(Halt)
XTHL(ExchangestacktopwithH-L)
SPHL(MovethecontentofH-Lpairtostackpointer)
EI (Enable Interrupt)
DI(Disable
Interrupt)**SIM**(SetInterru
ptMask)
RIM(ReadInterruptMask)
NOP(No Operation)

Govt.Polytechnic,Bhubaneswar

(Summer-2021)

Unit-3:TIMINGDIAGRAMS.

Faculty:Kanak PravaSwain, Lect.(ETC).

Subject:Microprocessor& Microcontroller.

Semester:4th Sem.ETC/IT.

:Defineopcode,operand,T-State,Fetchcycle,MachineCycle,Instructioncycle&discusstheconceptof timing diagram.

Opcode: Each instruction contains two parts, Operation code (Opcode) and operand. The first part of the instruction which specifies the task to be performed by the computer is called opcode.

Operand: The second part of the instruction is the data to be operated on and it is called operand. The operand may be 8-bit or 16-bit data, 8-bit or 16-bit data address. In some instructions the operand is implicit. When operand is a register the data is the content of the register.

Example:

MVI A,08

HereMVIisopcodeandA,08isoperand

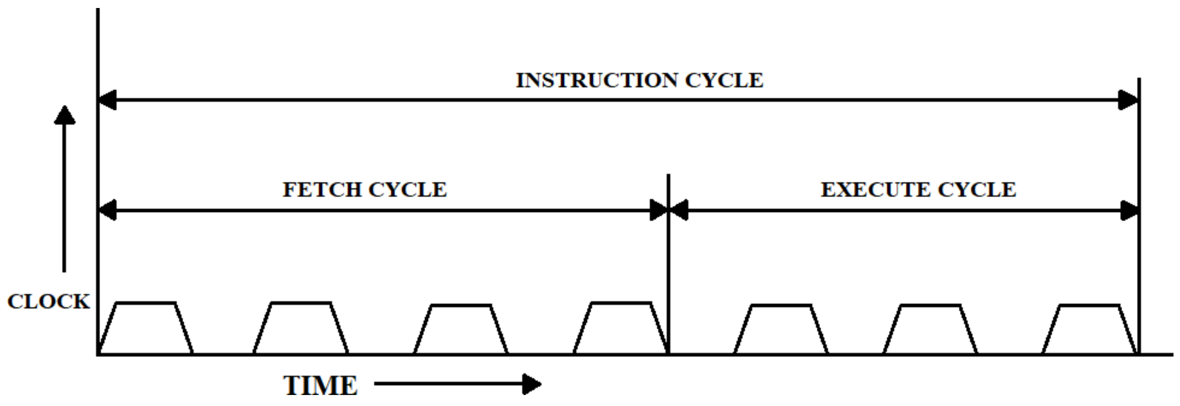
InstructionCycle:

ThenecessarystepsthataCPUcarriesouttofetchaninstructionand necessarydatafromthememoryand toexecuteit,constituteanInstructioncycle.AnInstructioncycleconsistsofafetchcycleandexecutecycle.

IC=FC+EC

Fetch Operation: The 1st byte ofan instructionisitsopcode. In the beginning of afetch cycle the content oftheprogramcounter,which istheaddressofthe memorylocationwhereopcode isavailable,issentto the memory.The entireoperationof fetching anopcode takes threeclock cycle. The clock cyclefor which the CPU waits is called wait cycle.

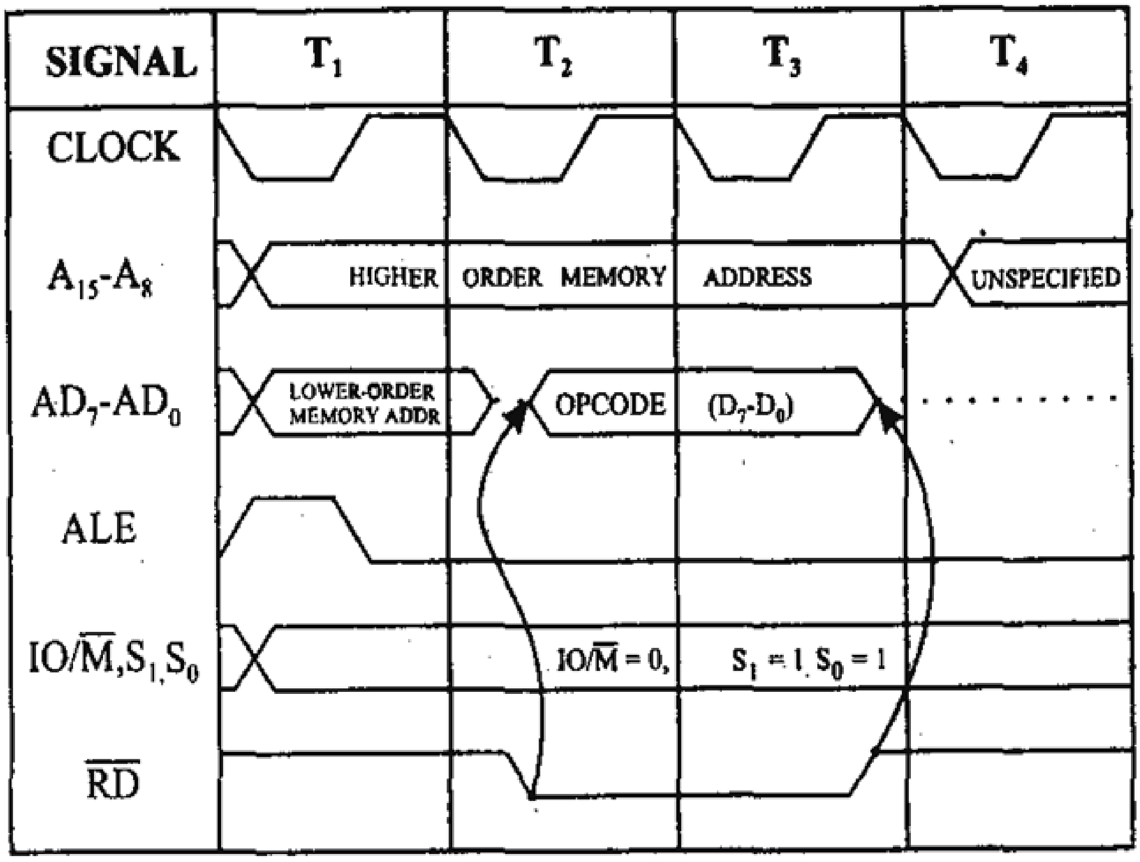
ExecuteOperation: Iftheoperandisinthegeneralpurposeregister,executionisimmediatelyperformed. Thetimetakenindecodingandexecutionisoneclockcycle.Areadcycleissimilartoafetchcycle.Inwrite cycle the data are sent from the CPU to memory.



Machine Cycle: The necessary steps carried out to perform the operation of accessing either memory or I/Odevice,constituteamachineCycle.i.enecessarystepscarriedouttoperformafetch,areadorawrite

operation constitute a Machine Cycle. In a machine cycle one basic operation such as opcode fetch, memory read, memory write, I/O read or I/O write is performed. An instruction cycle consists of several machine cycles.
T-State: OneSubdivisionofanoperationinoneclockcycleiscalledastateorT-State.

Timing Diagram:
The necessary steps which are carried out in a machine cycle can be represented graphically. Such a graphically representation is called **timing diagram.** The timing diagram for opcode fetch, memory read, memory write, I/O read or I/O write.
TimingDiagramforopcodeFetchCycle:
ForopcodefetchcycleT1,T2,T3,T4areconsecutivefourclockcycles.ThemicroprocessorissuesalowIO/M signal to indicate that it wants to make communicate with the memory. Again the microprocessor sends out high So & S1 signals to indicate that it is going to perform fetch operation.



During T1 the microprocessor sends out the address of the memory location where opcode is available. The16bitmemoryaddressissentthroughAddress/Data(AD)bus.8-MSBofthememoryaddressaresent through A8-A15 Busand 8-LSB of the memory address are sent through AS0-AD7 bus. It is used in time-multiplexedmode.Therefore,ithastobemadeavailabletocarrydataduringT2&T3.Themicroprocessor sendsanAddresslatchenablesignaltolatchthe8-LSBofthememoryaddress.DuringT2ADBusbecomes ready tocarry data.InT2microprocessor makesRDlow. During T3the opcode isplaced in theInstruction register IR which is within the microprocessor. The memory is disabled when RD goes high during T3. The fetch cycle is completed by T3. The opcode is decoded in T4.
If the instruction is 1-byte long, one machine cycle is required to fetch & execute the instruction. If the instruction is 2-byte or 3-byte long, it requires more machine cycle.

:Drawtiming diagramformemoryread,memorywrite,I/Oread,I/Owritemachine cycle.

Example:

TimingdiagramforMVI A,32

Thisinstructionis2-bytelongi.e3E,32.ItrequirestwomachinecycleM1&M2.ThefirstmachinecycleM1 is to fetch the operation code 3E from the memory and the second machine cycle M2 is for reading the data (05) from the memory. Fetch operation consist of 4 T-state and Memory Read operation consist of 3 T-State. So for MVI A,05 7 T-State & 2 Machine cycle is required.

ForFetchOperation:

ForopcodefetchcycleT1,T2,T3,T4areconsecutivefourclockcycles.ThemicroprocessorissuesalowIO/M signal to indicate that it wants to make communicate with the memory. Again the microprocessor sends out high So & S1 signals to indicate that it is going to perform fetch operation.

During T1 the microprocessor sends out the address of the memory location where opcode is available. The16bitmemoryaddressissentthroughAddress/Data(AD)bus.8-MSBofthememoryaddressaresent through A8-A15 busand 8-LSB of the memory address are sent through AS0-AD7 bus. It is used in time-multiplexedmode.Therefore,ithastobemadeavailabletocarrydataduringT2&T3.Themicroprocessor sendsanAddresslatchenablesignaltolatchthe8-LSBofthememoryaddress.DuringT2ADBusbecomes ready to carry data.In T2 microprocessor makesRDlow. During T3 the opcode isplaced in theInstruction register IR which is within the microprocessor. The memory is disabled when RD goes high during T3. The fetch cycle is completed by T3. The opcode is decoded in T4.

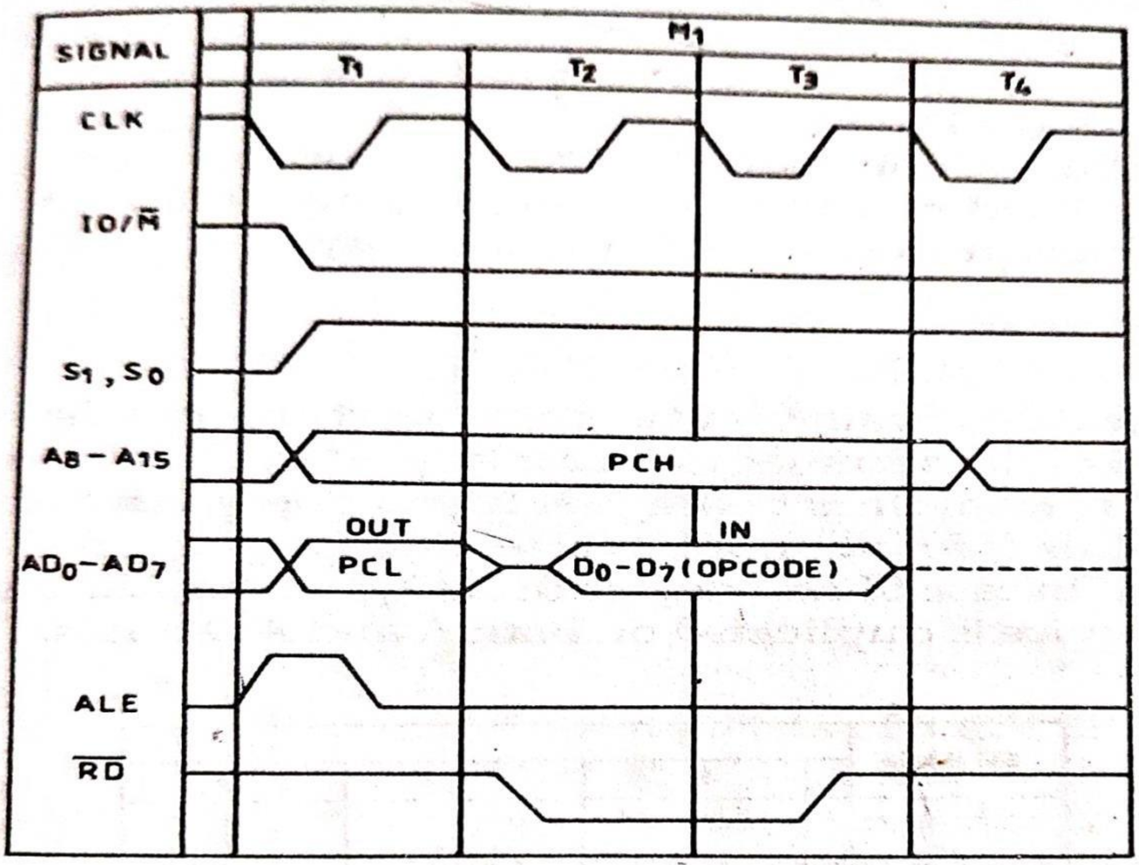


Fig. 3.9. Timing Diagram for Opcode Fetch Operation.

ForMemory Readoperation:

IO/M goes low indicating that the address is for memory. S1 & S0 are set to 1 & 0 respectively for read operation.OnA8-A158-MSBofthememoryaddressdata05aresent.DuringT18-LSBmemoryaddressof the data are sent on AD0-AD7.RD goes low in T2. In T3 data enters into the CPU. In T3 RD goes high and disables the memory.

In **memory write operation** instead of RD, WR goes low during T2 and goes high during T3 that the write operationisterminated.ThestatussignalS0andS1are1and0respectivelyforwriteoperation.ADbus is not disabled during T2.

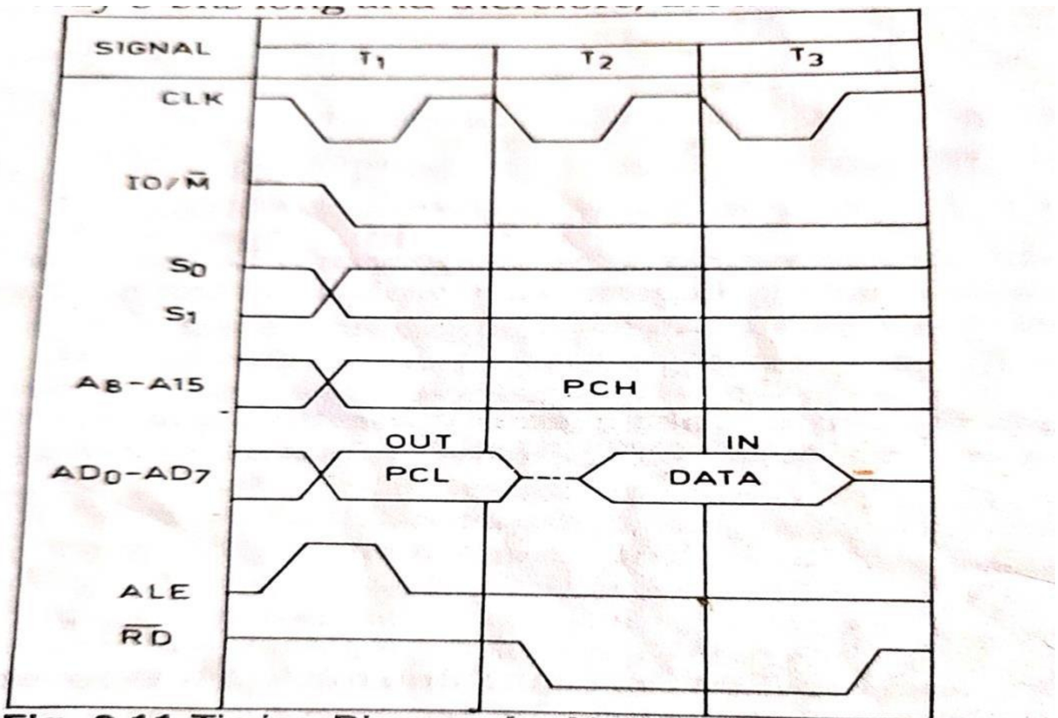


Fig. 3.11 Timing Diagram for Memory Read Operation.

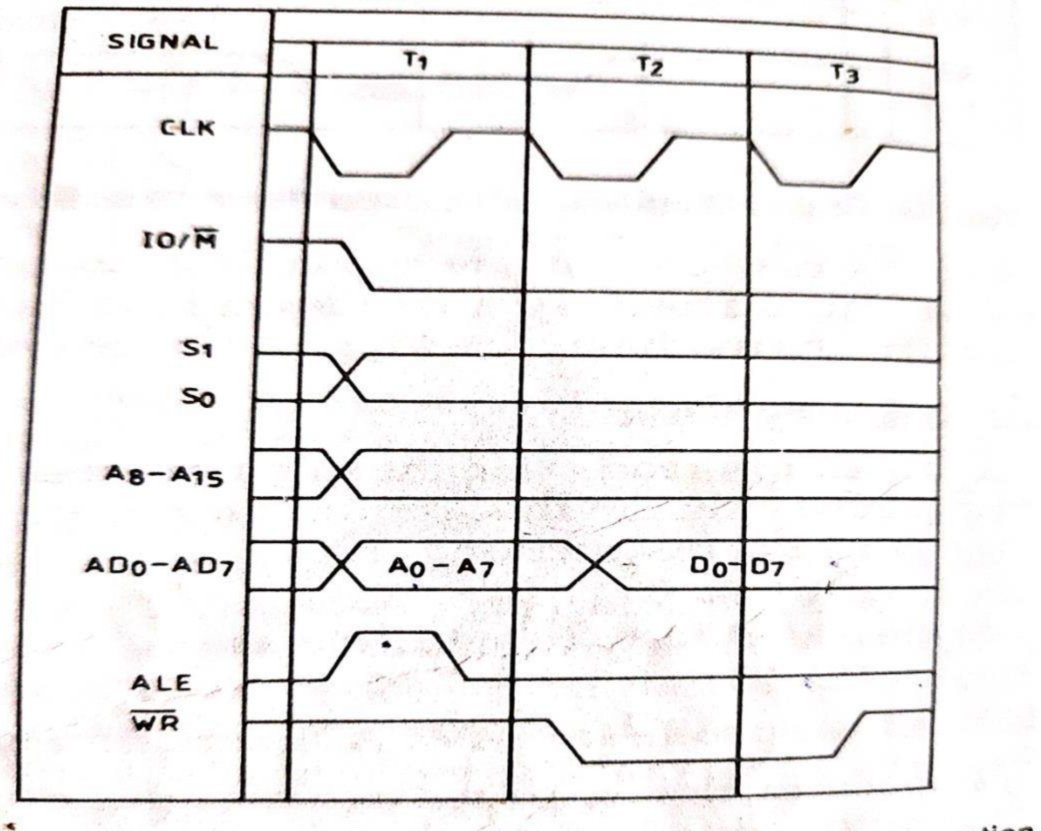


Fig. 3.12. Timing Diagram for Memory Write Operation.

I/OReadoperation: InI/OReadcyclethemicroprocessorreadsthedataavailableataninputportorinput device.AnI/OReadcycleissimilartomemoryreadcycle.TheonlydifferencebetweenI/OReadcycleand memory read cycleis thatIO/Msignalgoeshighin I/Oread cycle. Incase of I/O device theaddressis only 8-bit long and is duplicated on both A and AD buses.

The IN instruction is used for I/O read. It requires three machine cycle, fetch cycle, memory read cycle to read input port address and I/O read cycle to read the data from the port.

I/O write operation:

InI/O Writecyclethe CPU sends data toan I/O port fromthe accumulator.An I/O Writecycleis similar to memory Write cycle. The only difference between I/O Write cycle and memory read cycle is that IO/M signal goes high in I/O Writecycle. The address of the I/O port is duplicated on both A and AD buses.

The **OUT** instruction is used for I/O write. It requires three machine cycle, fetch cycle, memory read cycle for reading I/O device address from the memory and I/O write cycle for sending data to the I/O device.

<u>TimingDiagramforMOV,MVI,LDAinstruction</u>

1. **MOV:** **(byteinstruction/machinecycle/T-state)**

MOV	R,R	(1/1/4)	FetchOperation
MOV	M,R	(1/2/7)	Fetch,WriteOperation
MOV	R,M	(1/2/7)	Fetch,ReadOperation

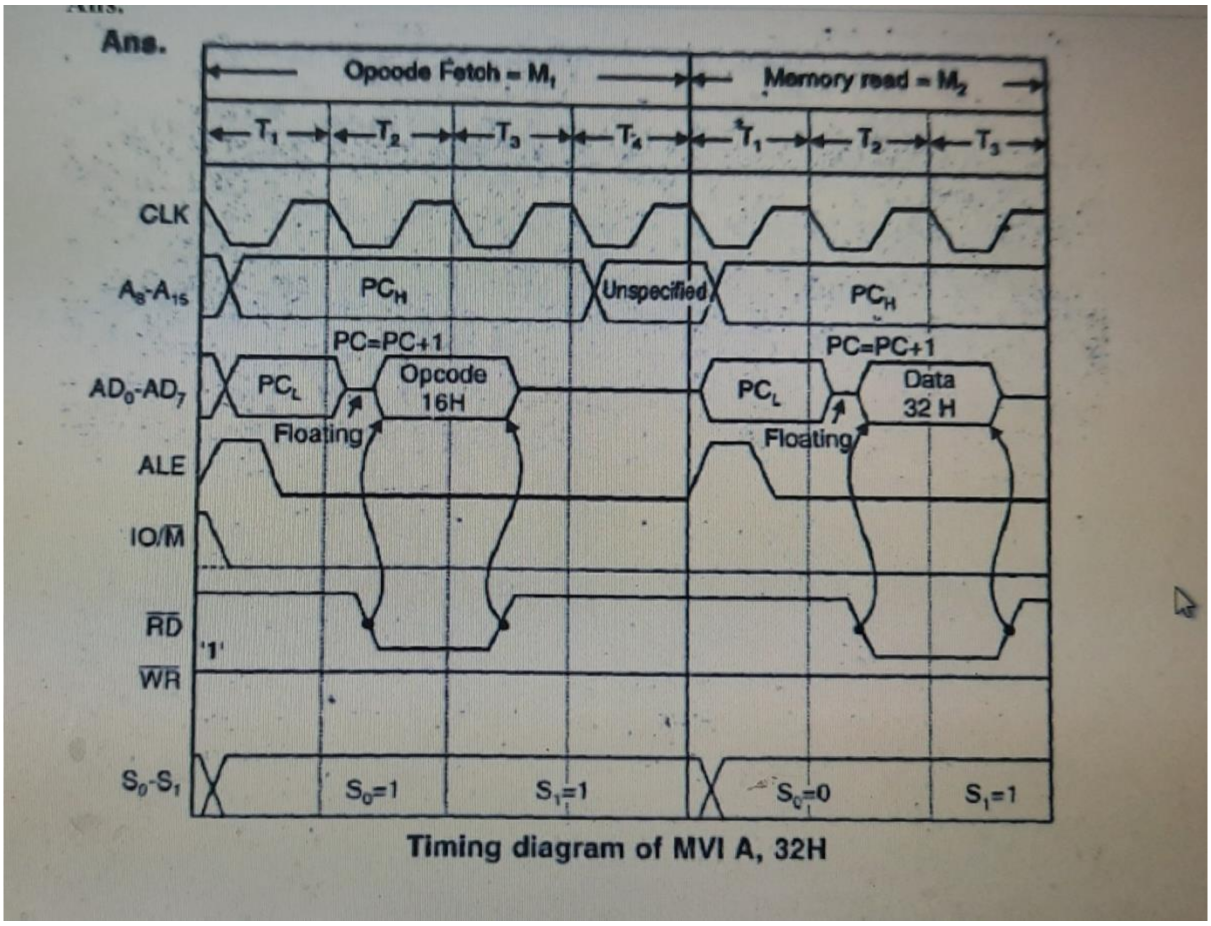
2. **MVI:** **(byteinstruction/machinecycle/T-state)**

MVI	R,data(2/2/7)	Fetch,ReadOperation
MVI	M, data(2/3/10)	Fetch,Read,Write Operation

3. **LDA:** **(byteinstruction/machinecycle/T-state)**

LDA	address(3/4/13)	Fetch,Read,Read,ReadOperation

:Drawaneatsketchforthetimingdiagramfor8085instruction(MOV,MVI,LDA instruction).



Timing diagram of MVI A, 32H

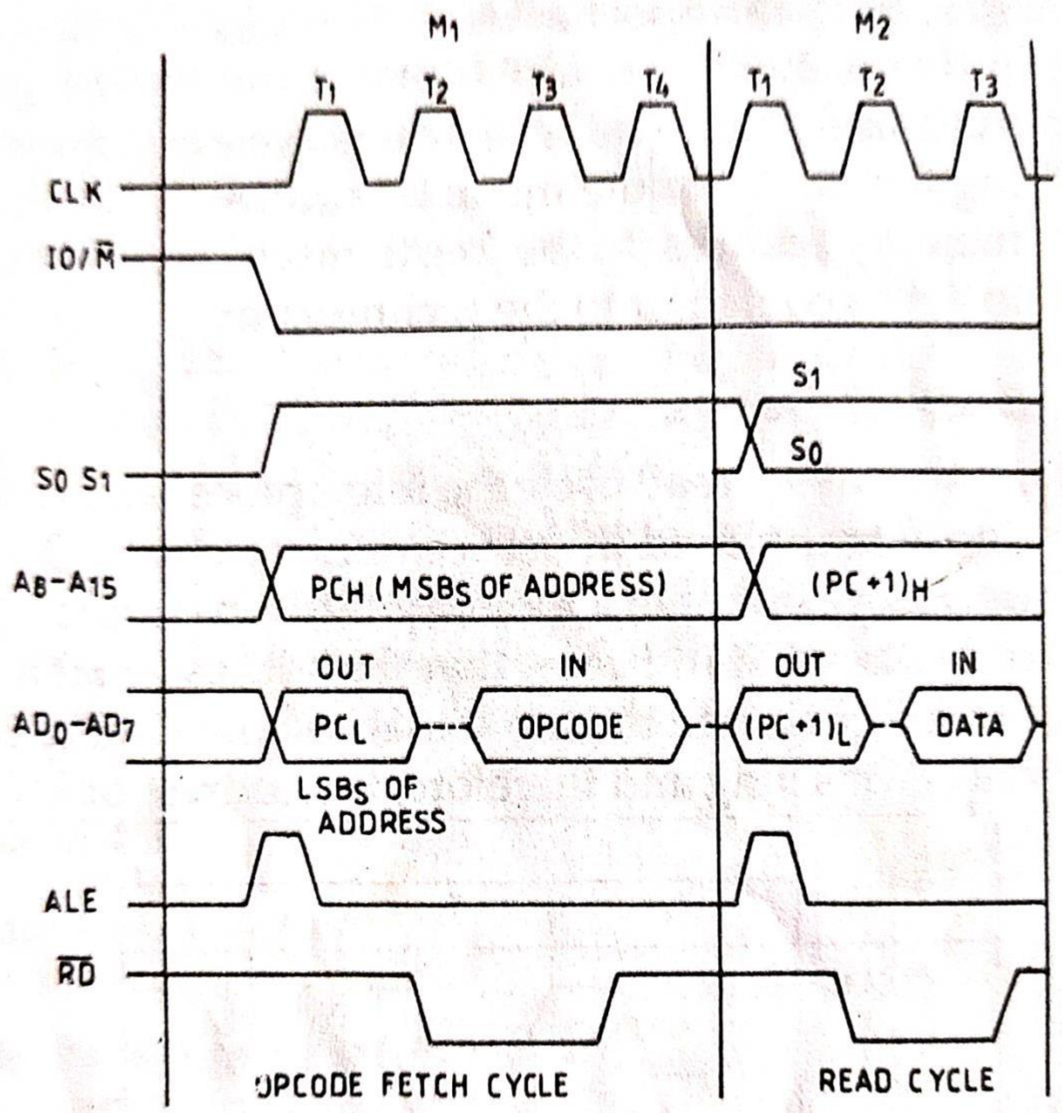


Fig. 3.10 Timing Diagram for MVI r, Data

Govt.Polytechnic,Bhubaneswar

(Summer-2021)

Unit-4:MicroprocessorBasedSystemDevelopmentAids

Faculty: Kanak Prava Swain, Lect.(ETC).

Subject:Microprocessor&Microcontroller.

Semester: 4th Sem.ETC/IT.

:Conceptofinterfacing.

Interfaceis the path for communication between two components. Interfacing is of two types, memory interfacing and I/O interfacing.

Peripheralsareconnectedtothemicrocomputerthroughelectroniccircuitsknownas**Interfacing**circuits.EachI/O device requires a separate interfacing circuit. The interfacing circuit converts the data available from the input device intocompatible format for the computer.Some of the general purpose single chip **interfacing devices** are

- I/Oport
- ProgrammablePeripheralInterface(PPI)
- DMAController
- InterruptController
- CommunicationInterface

SomeoftheSpecialpurpose**interfacingdevices** are

- CRT Controller
- FloppyDisk Controller
- KeyBoard&Displayinterface

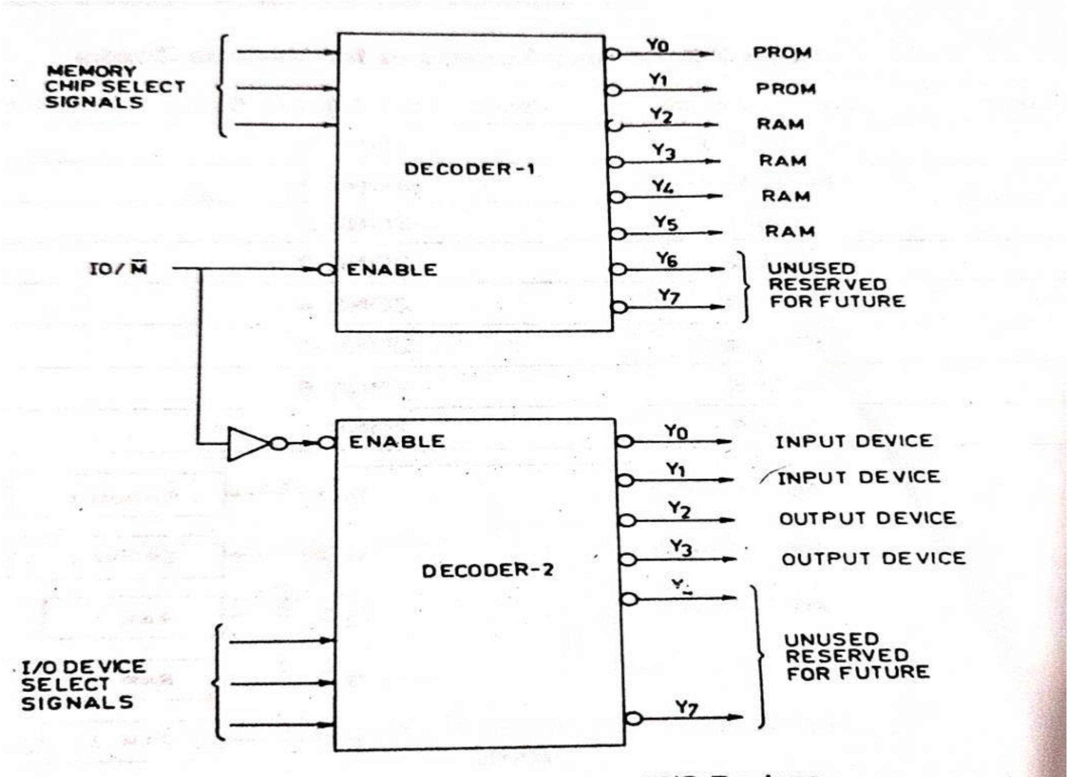


Fig. 7.2 Interfacing of Memory and I/O Devices.

InthediagramifI/O/M'ishighthe**decoder2**isactivatedandtherequiredI/Odeviceisselected.If I/O/M'islowthe **decoder1**isactivatedandtherequiredmemorychipisselected.

:DefineMapping &Data transfermechanisms-Memory mapping& I/OMapping.

Mapping:

Memory-**mapping** is a mechanism that **maps**a portion of a file, or**an**entire file, on disk to a range of addresses within **an** application's address space.

The Intel 8085 uses 16 bit address bus and it can access 2 16 =64 Kbytes. The 64 KB address are to be assigned to memory and I/O devices for their addressing. There are two schemes for the allocation of addresses to memory and input/ output devices.

- **MemorymappedI/Oscheme.**
- **I/O MappedI/O scheme.**

In Memory mapped I/O scheme there is only one address space. Some addresses are assigned to memories and some addresses to I/O devices. Suppose memory locations are assigned to the addresses 2000 to 24FF, any one of these addresses cannot be assigned to an I/O device. The addressesforI/Odevicesaredifferentfromtheaddresseswhichhavebeenassignedtomemories. **InI/O MappedI/O scheme** theaddressesassignedtomemorylocationcanalsobeassignedtoI/O devices. Since the same addresses assigned to memory location or an I/O devices, the microprocessor issue asignalthroughIO/Mtodistinguishwhether the address onthe address bus is for amemory location or I/O device.Whenthis **signal islow theaddressisformemory location** and if **it is high the address is for I/O device**. This scheme is used for large system.

DataTransferScheme:

Data transfer takes place between two devices such as microprocessor and memory, microprocessorandI/OdevicesandmemoryandI/Odevices.AcomputerhaveseveralI/Odevices of different speed. Aslow I/O devicecan not transfer data when microprocessor issuesinstruction for the same because it takes some time to get ready. Data transfer scheme are classified as

- **Programmeddatatransferscheme**
- **DMA(DirectMemoryAccess)DataTransferScheme**

<u>Programmeddatatransferscheme</u>arecontrolledbytheCPU.DataaretransferredfromI/Odevice toCPUorviceversaarecontrolofprogramme.TheProgrammeddatatransferschemeareclassified into

- SynchronousDatatransferscheme
- AsynchronousDatatransferscheme
- InterruptDrivenDatatransferscheme

SynchronousDatatransferscheme

Synchronous means at the same time, the device which sends data and the device which receives data are Synchronised with the same clock. When the CPU & I/O devices match in speed, this technique of the data transfer is employed.

AsynchronousDatatransferscheme

Asynchronous means at irregular interval. This technique of the data transfer is used when thespeedofI/Odevicedoesnotmatchthespeedofthemicroprocessor.Inthistechniquethestatus oftheI/Odevicei.ewhetherthedeviceisreadyornotischeckedbythemicroprocessorbeforethe data are transferred. When I/O device becomes ready, the microprocessor sends instruction to transferdata.Thismodeofdatatransferiscalledhandshakingmodeofdatatransferbecausesome signals are exchanged between the I/O device & microprocessor before the actual data transfertakes place.

DMA(DirectMemoryAccess)DataTransferScheme

In DMA data transfer scheme CPU does not participate. Data are directly transferred from an I/O device to memory or vice versa. The data transfer is controlled by the I/O device or a DMA controller. This scheme is employed when large amount of data are to be transferred.

An I/O device which wants to send data using DMA technique, sends the HOLD signal to the CPU. Onreceiving aHOLD signalfromanI/OdevicetheCPUgivesupthecontrolofbusesassoonasthe current machine cycle is completed.

DMA data transfer scheme is a faster scheme as compared to programmed data transfer scheme. It is used to transfer data from mass storage devices such as hard disks, floppy disks etc. It is also used for high speed printer.

:ConceptofMemoryInterfacing:-InterfacingEPROM&RAMMemories.

The address of the memory location or an I/O device is sent out by the microprocessor. The corresponding **memory** chip or I/O device is selected by a decoding circuit. The**interfacing** process includes matching the **memory** requirements with the microprocessor signals.

When we are executing any instruction, we need the microprocessor to access the **memory**for reading instruction codes and the data stored in the **memory**. For this, both the memory and the microprocessorrequiressomesignalstoreadfromandwritetoregisters. Theinterfacingcircuitshouldbe designed in such a way that it matches the memory signal requirements with the signals of the microprocessor.

8085InterfacingPins

Followingisthelistof8085pinsusedforinterfacingwithotherdevices−

- A_{15}-A_8(Higher AddressBus)
- AD_7- AD_0(LowerAddress/DataBus)
- ALE
- RD
- WR
- READY

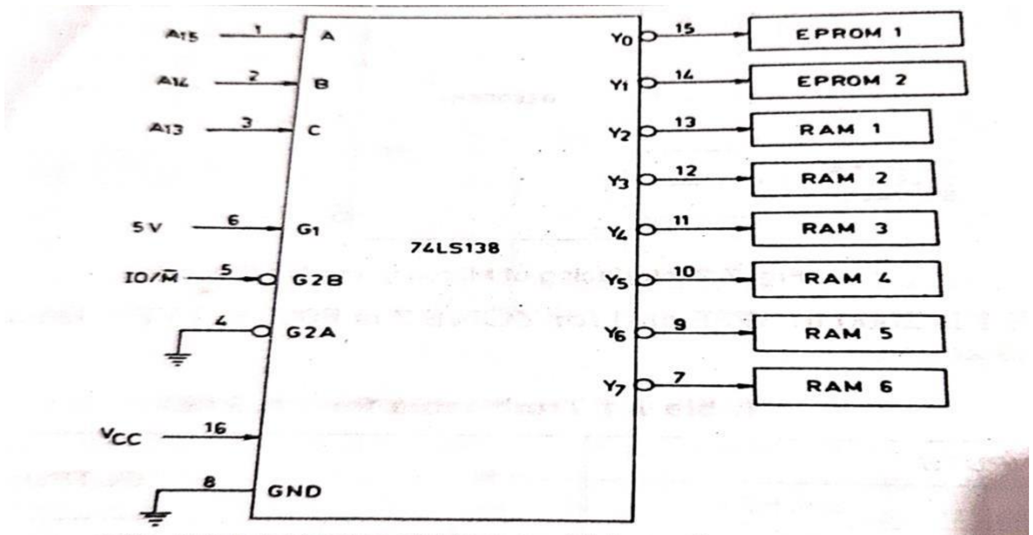


Fig. 7.3 Interfacing of Memory Chips using 74LS138.

:ConceptofAddressdecodingforI/Odevices.

Address decoding refers to the way a computer system **decodes** the **addresses** on the **address** bus to select memory locations in one or more memory or peripheral devices .... Infull**addressdecoding**,eachaddressable memorylocation correspondstoaunique**address**valueonthe**address**bus.

There are various communication devices like the keyboard, mouse, printer, etc. So, we need to interface the keyboardandotherdeviceswiththemicroprocessorbyusinglatchesandbuffers.Thistypeofinterfacingisknown as I/O interfacing.

Thetransferofdatabetweenkeyboardandmicroprocessor,andmicroprocessoranddisplaydeviceiscalledInput OutputInterfacing8085MicroprocessororI/Odatatransfer.ThisdatatransferisdonewiththehelpofI/Oports.

Therearetwowaysofcommunicationinwhichthemicroprocessorcanconnectwiththeoutside world.

- SerialCommunicationInterface
- ParallelCommunicationinterface

SerialCommunicationInterface−Inthistypeofcommunication,theinterfacegetsasinglebyteofdatafromthe microprocessorandsendsitbitbybittothe other systemseriallyandvice-a-versa.

Parallel Communication Interface − In this type of communication, the interface gets a byte of data from themicroprocessorandsendsitbitbybittotheothersystemsinsimultaneous(or)parallelfashionandvice-a-versa.

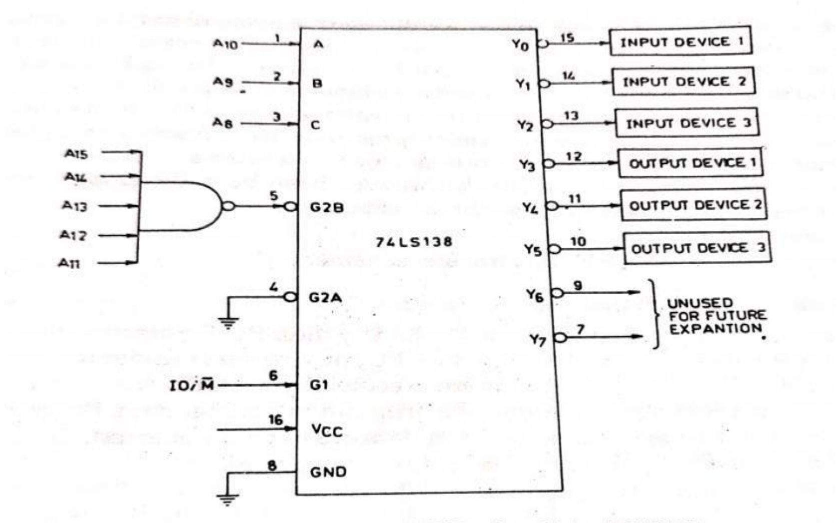


Fig. 7.4 Interfacing of I/O Devices Using 74LS138.

Table 7.2 Memory Locations for Various Zones

Decoder Output	Memory Device	Zones of the Address Space	Memory Locations Address
Y_0	EPROM 1	ZONE 0	0000 to 1FFF
Y_1	EPROM 2	ZONE 1	2000 to 3FFF
Y_2	RAM 1	ZONE 2	4000 to 5FFF
Y_3	RAM 2	ZONE 3	6000 to 7FFF
Y_4	RAM 3	ZONE 4	8000 to 9FFF
Y_5	RAM 4	ZONE 5	A000 to BFFF
Y_6	RAM 5	ZONE 6	C000 to DFFF
Y_7	RAM 6	ZONE 7	E000 to FFFF

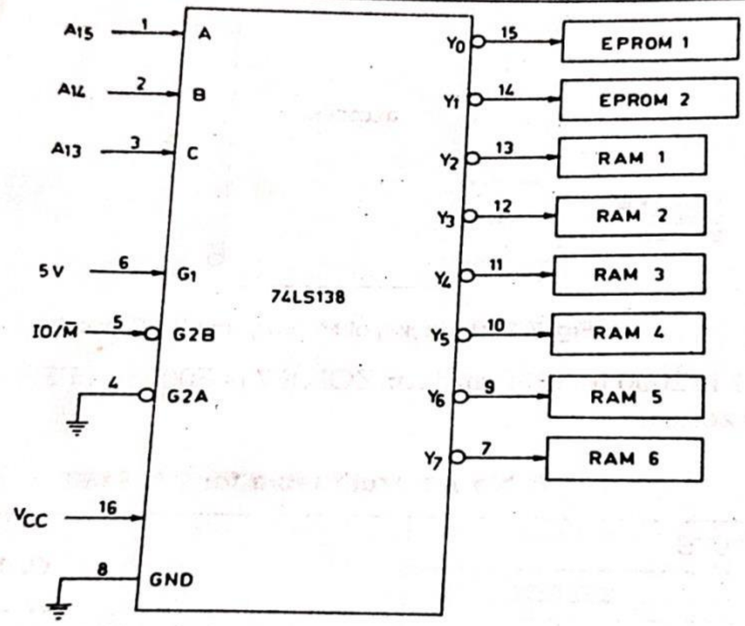


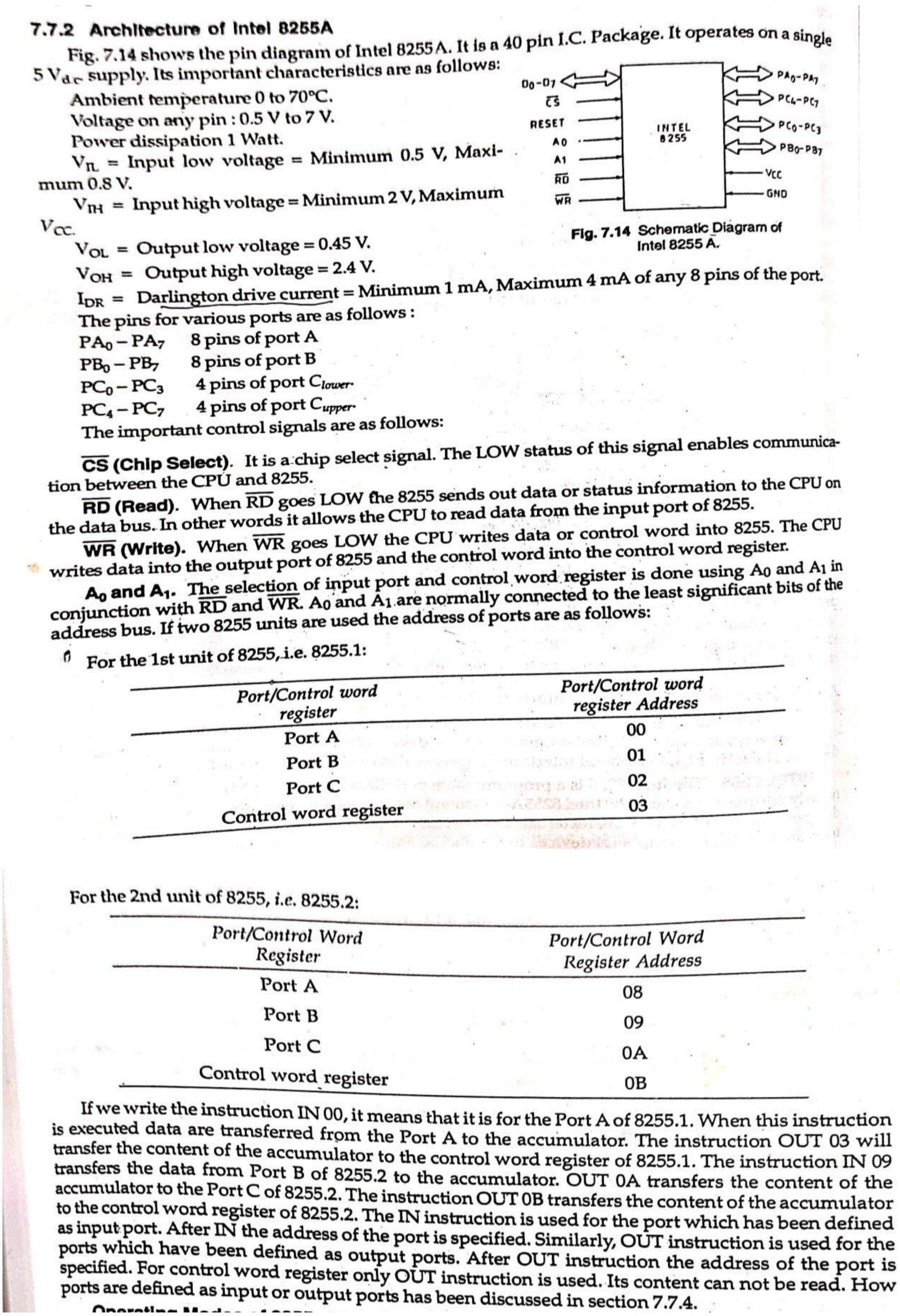
Fig. 7.3 Interfacing of Memory Chips using 74LS138.

:ProgrammablePeripheralInterface: 8255.

ProgrammablePeripheralInterface(PPI)(Intel8255):

A Programmable Peripheral Interface (PPI) is a multiport device. The main function are to interface peripheral devices tothe microcomputer. It has three 8-bit port namelyPort-A, Port-B, Port-C. Port-Chas beendividedintotwo4-bitportsnamely Port-Cu(upper) andPort-Cl(lower).Totaltwo8-bitportandtwo 4-bit ports are available and it can be programmed either as an input port or output port.

ArchitectureofIntel-8255:



7.7.2 Architecture of Intel 8255A

Fig. 7.14 shows the pin diagram of Intel 8255A. It is a 40 pin I.C. Package. It operates on a single 5 V_{dc} supply. Its important characteristics are as follows:

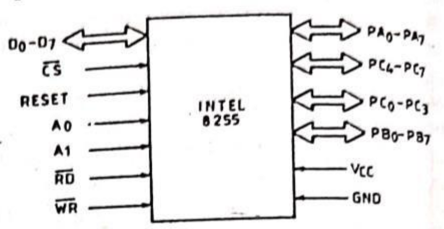


Fig. 7.14 Schematic Diagram of Intel 8255 A.

Ambient temperature 0 to 70°C.
Voltage on any pin : 0.5 V to 7 V.
Power dissipation 1 Watt.
V_{IL} = Input low voltage = Minimum 0.5 V, Maximum 0.8 V.
V_{IH} = Input high voltage = Minimum 2 V, Maximum V_{CC}.
V_{OL} = Output low voltage = 0.45 V.
V_{OH} = Output high voltage = 2.4 V.
I_{DR} = Darlington drive current = Minimum 1 mA, Maximum 4 mA of any 8 pins of the port.
The pins for various ports are as follows :

$PA_0 - PA_7$	8 pins of port A
$PB_0 - PB_7$	8 pins of port B
$PC_0 - PC_3$	4 pins of port C_{lower}.
$PC_4 - PC_7$	4 pins of port C_{upper}.

The important control signals are as follows:

$\overline{CS}$ (Chip Select). It is a chip select signal. The LOW status of this signal enables communication between the CPU and 8255.

$\overline{RD}$ (Read). When $\overline{RD}$ goes LOW the 8255 sends out data or status information to the CPU on the data bus. In other words it allows the CPU to read data from the input port of 8255.

$\overline{WR}$ (Write). When $\overline{WR}$ goes LOW the CPU writes data or control word into 8255. The CPU writes data into the output port of 8255 and the control word into the control word register.

A_0 and A_1. The selection of input port and control word register is done using A_0 and A_1 in conjunction with $\overline{RD}$ and $\overline{WR}$. A_0 and A_1 are normally connected to the least significant bits of the address bus. If two 8255 units are used the address of ports are as follows:

(i) For the 1st unit of 8255, i.e. 8255.1:

Port/Control word register	*Port/Control word register Address*
Port A	00
Port B	01
Port C	02
Control word register	03

For the 2nd unit of 8255, *i.e.* 8255.2:

Port/Control Word Register	*Port/Control Word Register Address*
Port A	08
Port B	09
Port C	0A
Control word register	0B

If we write the instruction IN 00, it means that it is for the Port A of 8255.1. When this instruction is executed data are transferred from the Port A to the accumulator. The instruction OUT 03 will transfer the content of the accumulator to the control word register of 8255.1. The instruction IN 09 transfers the data from Port B of 8255.2 to the accumulator. OUT 0A transfers the content of the accumulator to the Port C of 8255.2. The instruction OUT 0B transfers the content of the accumulator to the control word register of 8255.2. The IN instruction is used for the port which has been defined as input port. After IN the address of the port is specified. Similarly, OUT instruction is used for the ports which have been defined as output ports. After OUT instruction the address of the port is specified. For control word register only OUT instruction is used. Its content can not be read. How ports are defined as input or output ports has been discussed in section 7.7.4.

Intel8255isa40pinI.Cpackage andoperatesin+5Vregulatedpowersupply.

- **PA0– PA7–** Pinsof port A
- **PB0– PB7–** Pinsof port B
- **PC0– PC7–** Pins of portC
- **D0– D7–**Datapins forthe transferof data
- **RESET–**Resetinput
- **RD’–**Read input

- **WR'–**Writeinput
- **CS'–** Chipselect
- **A1andA0 –**Addresspins

OperatingModesof8255:

8255Ahasthreedifferentoperatingmodes−

- **Mode 0 Simple Input/output** − In this mode, Port A and B is used as two 8-bit ports and Port C as two 4-bitports. Each portcanbe programmedin either inputmodeor output modewhereoutputsarelatched and inputs are not latched. Ports do not have interrupt capability.
- **Mode 1 Strobed Input/output** − In this mode, Port A and B is used as 8-bit I/O ports. They can be configured as either input or output ports. Each port uses three lines from port C as handshake signals. Inputs and outputs are latched.
- **Mode 2Bidirectional Port**− In this mode, Port A can be configured as the bidirectional port and Port B either in Mode 0 or Mode 1. Port A uses five signals from Port C as handshake signals for data transfer. The remaining three signals from Port C can be used either as simple I/O or as handshake for port B

Control Word For8255:

A control word is formed which contains the information regarding the function and modes of the ports. TheCPUoutputsthecontrolwordto8255.Accordingtotherequirementaportcanbeprogrammedtoact eitherInputportoroutputport.Forprogrammingtheportsof8255acontrolwordisformed.Controlword is written into the control word register which is within 8255.

Bit no 0-Itis forPortC-lowerTomake Inputitis setto1
TomakeOutputitissetto0

Bitno1-ItisPort B TomakeInputitissetto1
TomakeInputitissetto1

Bitno 2-ItisMode ofPortBFor Mode0itissetto0
ForMode 1itissetto1

Bit no 3-Itis forPortC-upperTomake Inputitis setto1
TomakeOutputitissetto0

Bit no4-Itis forPort A TomakeInputitissetto1
TomakeOutputitissetto0

Bitno5,6-Itis Modeof PortA

ModeofPortA	**Bitno 5**	**Bitno 6**
Mode-0	0	0
Mode-1	0	1
Mode-2	1	0or 1

Bit no 7- It is set to 1, If Port A,B,C are defined as input/output port.
Itissetto0,Ifindividualpinof portCaretobesetorreset.

7	6	5	4	3	2	1	0

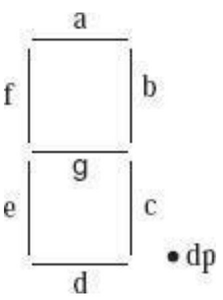
Bitnoofcontrolword.

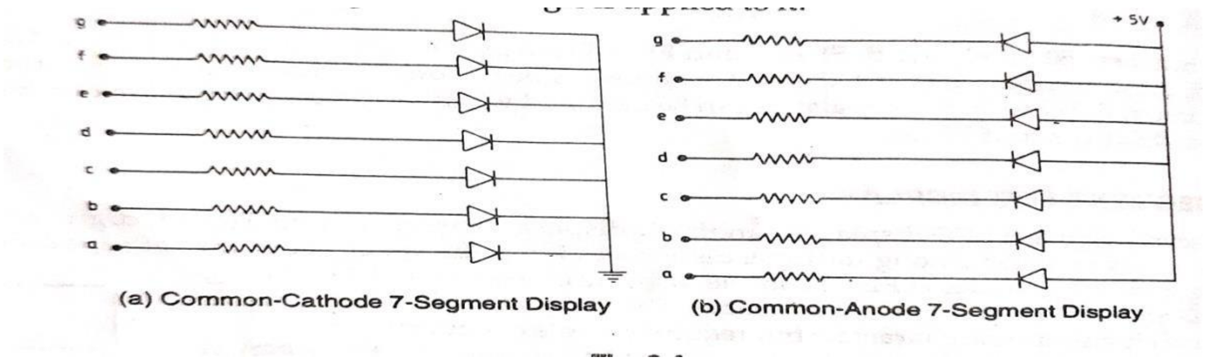
:ADC&DACwithInterfacing.

:InterfacingSevenSegmentDisplays

The**7-segment LED display** is a multiple display. It can display 0-9 numeric, alphabetic. Each**LED**has a negativelegthatisconnectedtooneofthepinsofthe device.EachLEDcanbecontrolledseparately.Todisplaya digit or letter the desired segments are made ON.

Anoutputdevicewhichisverycommonis,especiallyinthekitof8085 microprocessoranditistheLightEmitting Diode consisting of seven segments. We denote the segments as a, b, c, d, e, f, g.Moreover, these are LEDs or together a series of Light Emitting Diodes. a 7-segment display is as shown in the following Fig.

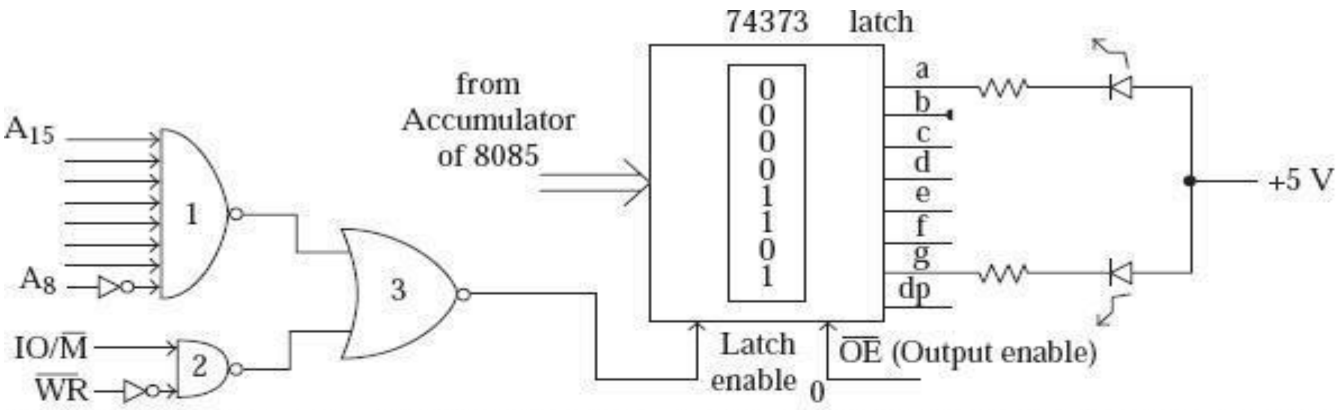



g
f
e
d
c
b
a
+5V
(a) Common-Cathode 7-Segment Display
(b) Common-Anode 7-Segment Display

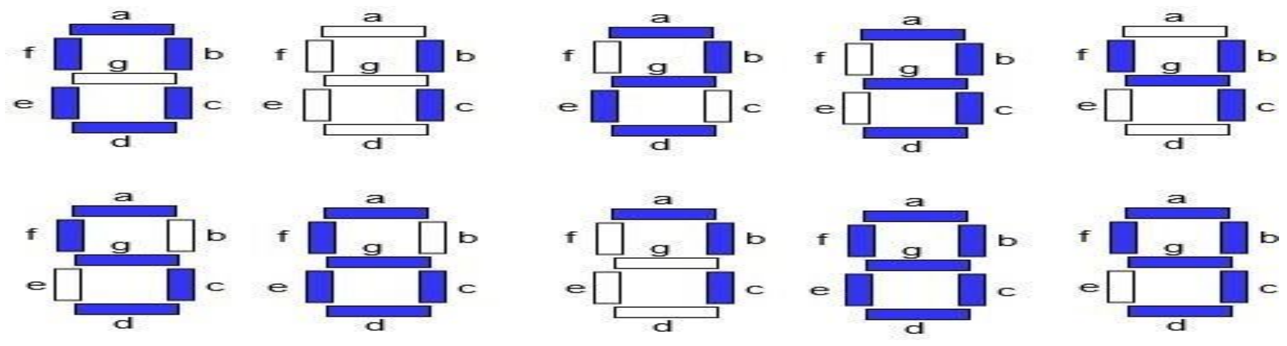
There are two types of 7-segment LED: They are the **common anode type** and the **common cathode type**. In commonanode typedisplayallthe7anodesofLEDsaretiedtogether totheground.When+5vdcappliedtoany segment, the corresponding diode emits light. Incommon cathode type display all the 7 anodes of LEDs are tied together to the ground. When +5v dc applied to any segment, the corresponding diode emits light.

The 7-segment displays are not connected to I/O port directly. They are connected through drivers/decoders.

Theuseof74373latchforinterfacinga7-segmentdisplayisshownin thefollowing Fig.



Note: To keep the figure simple, only two of the eight segment connections are shown. The other six segment connections are similar.



In the 74373 latch is used as an I/O mapped I/O port with the port address as FE H. This could be easily verified fromthechipselectcircuitusedinthefigure.Thefollowinginstructionsaretobeexecutedtodisplaycharacter‘3’ on the 7-segment display. The corresponding program to send 0D H to the port FE H will be -

MVIA,0DH OUT

FE H

UsingMVIinstructionweareinitializingAccumulator(A)withByte0D Hi.e.00001101. Thenitwill besenttothe port FE H by the instruction OUT.

ApplicationsofSevenSegment Displays

Commonapplicationsofsevensegmentdisplaysarein:

- Digital clocks
- Calculators
- Wristwatchers
- Speedometers
- Motor-vehicleodometers
- Radiofrequencyindicators
- Microwaveorfancytoaster ovens

:Generatesquarewaveson all linesof 8255.

Inthissectionyouwillseetheassembly languagecodetogenerateSquarewaveusing8085 microprocessor:

Atfirstweassumethat,CWRaddressof8255is0BandSOC pinof0808isconnectedto0thpinof PORT B MVI A,89H

```
OUT0BH
MVIA,01H
OUT 09H

BACK:MVIA,FFH OUT
08H
MVI C,BOH
LOOP1:DCRC
JNZLOOP1
MVI A,00H
OUT 08H
MVIC,B0H

LOOP2:DCRC
JNZ LOOP2
JMP BACK
```

:DesignInterfaceatrafficlightcontrolsystemusing8255.

For microprocessor based **traffic light control**, all ports of 8255 have been programmed as output ports. The control word to make all ports output ports in Mode 0 operation is 80H. The connection of pins of the ports to LED have been made through buffers (7407).Positive logic has been used to switch on LEDs. Three types of LEDs have been used **Red, Yellow and Green**. Green light glows to allow crossing, yellow to make alert and red does not allow crossing.

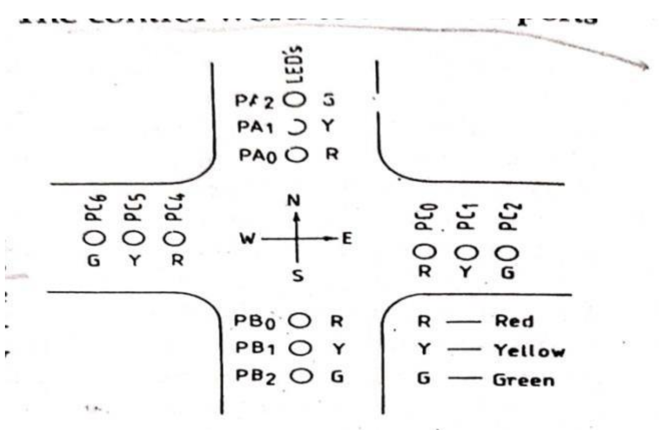


Fig. 9.54. Traffic Light Control.

Memory Address	Machine codes	Labels	Opcode	Operands	Comments
4100	3E,80		MVI	A,80H	GetControlwordfor8255.
4102	D3,0B		OUT	0B	InitializePort 8255.
4104	3E,01	LOOP	MVI	A,01	
4106	D3,09		OUT	09	**REDON**forSouth.
4108	D3,08		OUT	08	**REDON**forNorth.
410A	3E,44		MVI	A,44	**GREEN ON**foreastandwest.
410C	D3,04		OUT	0A	
410E	CD,00,42		CALLDELAYI		
4111	3E,22		MVIA,22		**YELLOW ON**for eastandwest.
4113	D3,0A		OUT0A		
4115	3E,02		MVIA,02		
4117	D3,09		OUT09		**YELLOW ON**for South.
4119	D3,08		OUT08		**YELLOW ON**for North.
411B	CD,13,42		CALLDEPLAYII		
411E	3E,11		MVIA,11		
4120	D3,0A		OUT0A		**REDON**for eastand west.
4122	3E,04		MVIA,04		
4124	D3,08		OUT08		**GREEN ON**for north.
4126	D3,09		OUT09		**GREEN ON**for south.
4128	CD,00,42		CALLDELAYI		
412B	3E,22		MVIA,22		**YELLOW ON**for eastandwest.
412D	D3,0A		OUT 0A		
412F	3E,02		MVIA,02		
4131	D3,09		OUT09		**YELLOW ON**for South.
4133	D3,08		OUT08		**YELLOW ON**for North.
4135	CD,13,42		CALLDEPLAYII		
4138	C3,04,41		JMPLOOP		

DELAYI

4200	06,20		MVIB,20H
4202	0E,FF	G03	MVIC,FF
4204	16,FF	G02	MVID,FF
4206	15	G01	DCR D
4207	C2,06,42		JNZG01
420A	0D		DCRC
420B	C2,04,42		JNZG02
420E	05		DCR B
420F	C2,02,42		JNZG03

```
        4212          C9                RET
DELAYII
        4213          06,10             MVIB,10
        4215          C3,02,42          JMP 4202          G03
```

:Design interfaceforsteppermotorcontrolusing 8255.

Asteppermotorrotatesinstepsinresponsetodigitalpulseinputs.Theshaftofthemotorrotatesinequal to increments when a train of input pulses is applied. To control the direction and number of steps appropriate pulsesareappliedtothestarterwindingsofthemotor.Therearetwotypesofsteppermotor**a.PermanentMagnet Typeb. Variable reluctance Type.**

The Permanent magnet type stepper motor consists of four pole stator and a rotor with six permanent poles.Thestatorwindingsareenergisedbypulses.Themotorhasfourphaseexcitationastherearefourpoleson thestator.Eachpolehastwocoilwoundintheoppositesensesothatthepolecanbemadeeitheranorthpoleor a south pole.

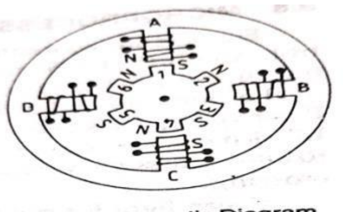


Fig. 9.51. Schematic Diagram of Stepper Motor.

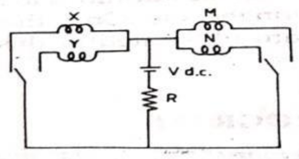


Fig. 9.52. Bifiller Pole Winding

Here X and y are two coils on the same pole. M and n are also the coils on the same pole situated at diametrically opposite position.Resistance R is used to reduce the electrical inertia of the highly inductive windings. The motor is known as bifiller wound stepper motor.

IfthepoleAismadenorthpole,poleC ismadesouthpole. Thepermanentsouthpoleno1oftherotor willstandjustbelowpoleAofthestator. TogiveaclockwisemotionthesupplyofthepoleAandCisswitchedoff and the pole B and D are energised. The pole B is made south pole and D is north pole.

Now the permanent north pole no 2 of the rotor comes just below the pole B.In the next step pole C is made an N-pole and Ais S-pole. After thisD is madeS-pole and B is N-pole.Again poleA is N-pole andC is S-pole and the whole sequence is repeated. In this process poles are energised togive a clockwise rotation.

Torotate therotoranticlockwisemaking ApoleanN-poleandC poleaS-pole,D ismadeS-poleandBis N-pole.

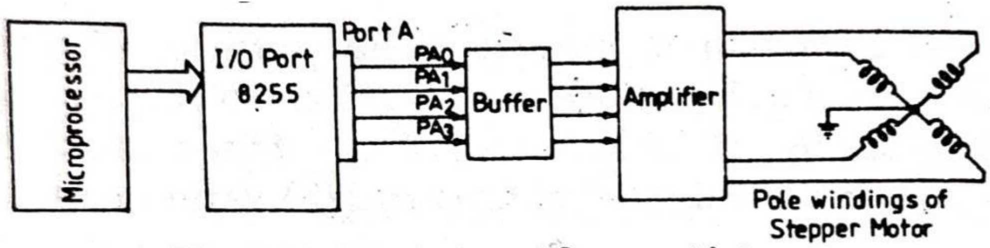


Fig. 9.53. Interfacing of Stepper Motor.

For interfacing connections of stepper motor, 12 V dc supply is used to energise the poles. Pulses sent by themicroprocessorswitchonratedvoltagetothewindingsofthedesiredpoles.Afterenergisingonesetofthe pole windings some delay is provided, then power supply is switched on to the other set of pole windings. This delay time governs the speed of the motor.

:BasicconceptofotherInterfacingDMAcontroller,USART. DMA Controller:

The bulk data transfer from I/O devices to the memory or from the memory to I/O devices through the accumulatorisatimeconsumingprocess.Forsuchasituation **DirectMemoryAccess(DMA)**techniqueisused.In DMA data transfer scheme, data are directly transferred from an I/O devices to the memory and vice versa.

Intel8257isaProgrammableDMAController.Itis 40pin IC packageandrequires5vsupplytooperate.FourI/O devices can be interfaced to the microprocessor through this device.

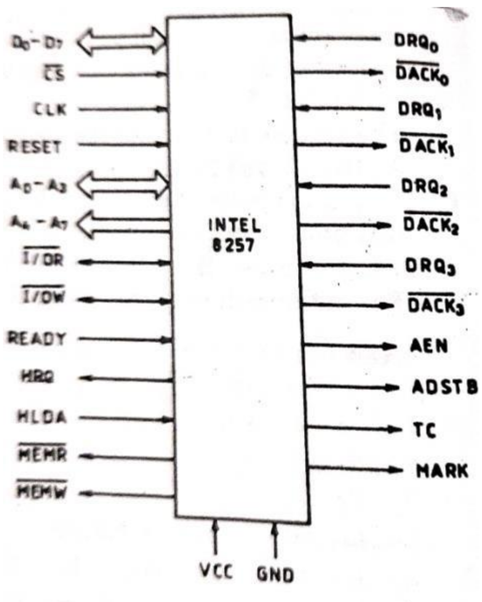


Fig. 7.24 Schematic Diagram of Intel 8257.

ItiscapableofperformingthreeoperationsRead,WriteandVerify.DuringtheReadoperationthedataaredirectly transferredfromthememorytotheI/Odevice.DuringWriteoperationthe dataaredirectlytransferredfromthe memory to the I/O device. On receiving a request from the I/O device, 8257 generates a sequential memory address which allow I/O device to Read or Write directly to or from the memory.

USART:(ProgrammableCommunicationInterface(PCI)Intel8251)

The Intel 8251 is a Programmable Communication Interface. It is Universal Synchronous/ Asynchronous Receiver/ Transmitter **(USART)**. It is compatible with 8085,8086 etc. The 8251 can be used to transmit/ receive serial data. It accepts data in parallel format from the microprocessor and converts them into serial data for transmission.

Govt.Polytechnic,Bhubaneswar

(Summer-2021)

Unit-5:Microprocessor(ArchitectureandProgramming-8086-16bit) Faculty:

Kanak Prava Swain, Lect.(ETC).

Subject:Microprocessor&Microcontroller.

Semester: 4th Sem.ETC/IT.

:RegisterOrganisationof8086.

Intel8086containsthefollowingregisters

a. GeneralPurposeRegisters.
b. PointerandIndexRegisters.
c. Segment Registers.
d. InstructionPointer.
e. StatusFlags.

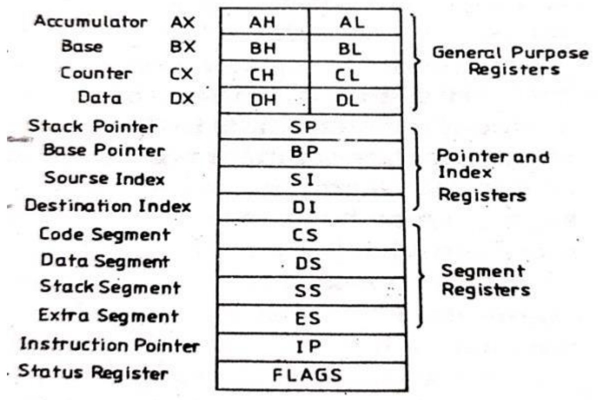


Fig. 11.3 Register organization of Intel 8086

:Internal Architectureof8086.

<u>FunctionalUnitorBlockDiagramofIntel8086:</u>

Intel 8086 is a 16 bit N channel HMOS microprocessor. HMOS is used for High Speed MOS. It is a 40 pin IC package and it is Dual In-line Package(DIP). It has 20 address lines, it candirectly address up to 2 to the power 20 =**1 MB** of memory. The 16 loworderaddresslinesaremultiplexedwithdataBusand4highorderaddresslinesaretimemultiplexedwithstatussignals. 8 LSB of data are transmitted on AD0-AD7 and 8 MSB of data on AD8-AD15.

8086containstwoindependent functionalunits:**aBusInterfaceUnit(BIU)**andan**ExecutionUnit(EU)**.

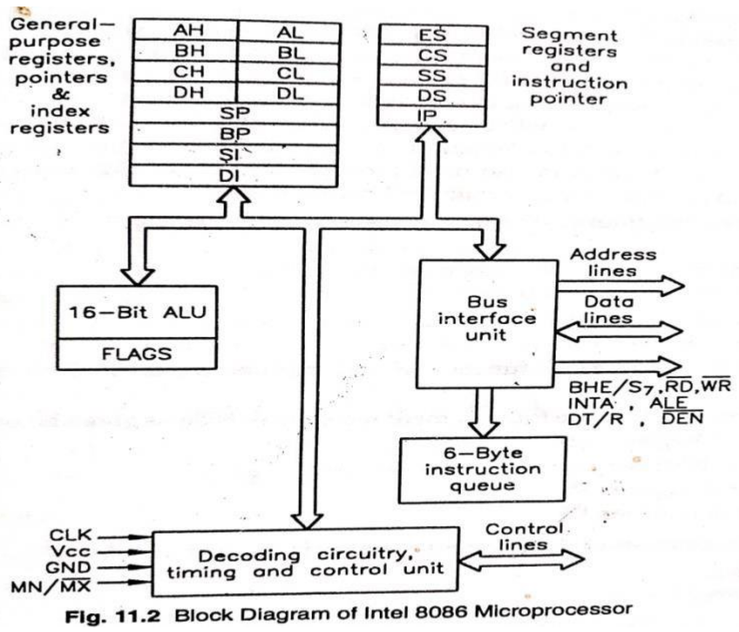


Fig. 11.2 Block Diagram of Intel 8086 Microprocessor

BusInterfaceUnit (BIU)
Thesegmentregisters,instructionpointerand 6-byteinstructionqueueareassociated withthe**BusInterfaceUnit(BIU) The Bus**

Interface Unit (BIU) :

- Handlestransferofdataandaddressesbetweenprocessor,memory/IOdevices,
- Fetchesinstructioncodes,storesfetchedinstructioncodesinfirst-in-first-outregistersetcalleda**queue**,
- ReadsdatafrommemoryandI/O devices,
- WritesdatatomemoryandI/Odevices,
- Itrelocatesaddressesof operands sinceitgetsun-relocatedoperandaddressesfromEU.TheEUtellsthe BIU from where to fetch instructions or where to read data.

ExecutionUnit (EU):
TheGeneralpurposeregisters,StackPointer,BasePointer, andIndexRegister,ALU,FlagRegister,Instructiondecoder,and timing & control unit constitute **Execution Unit (EU).**

- The**EU** receivesopcodeofaninstructionfromthequeue,decodesitandthenexecutesit.WhileExecution, unitdecodesorexecutesaninstruction,thentheBIUfetchesinstructioncodesfromthememoryandstores them in the queue.
- The **BIU and EU** operate in parallel independently. While **EU** executes instructions, the **BIU** fetches instructions.Thistypeofoverlappedoperationofthefunctionalunitofamicroprocessoriscalled**Pipelining**. This makes processing faster.

GeneralPurposeRegisters: Therearefour16-bitgeneralpurposeregisters:

- AX
- BX
- CX
- DX.

Eachofthese16-bitregistersarefurthersubdividedinto8-bitregistersIthasthefollowingfunctional parts:

16bit Registers	**8-bitHighorderRegisters**	**8-bitLoworderRegisters**
AX	AH	AL
BX	BH	BL
CX	CH	CL
DX	DH	DL

TheRegisterAXservesasanaccumulator,BX,CX,DXareusedasGeneralpurpose register.

PointerandIndexRegister:

- **InstructionPointer(IP):** Theinstructionpointerinthe8086microprocessoractsasa **programcounter**.Itindicates to the address of the next instruction to be executed.

- **IndexRegister:**Thefollowingfour registersareinthegroupofpointerandindexregisters:
  - StackPointer (SP)
  - BasePointer (BP)
  - SourceIndex (SI)
  - DestinationIndex(DI)

- **InstructionQueue:** WhenEUexecutesinstructions,theBIUgets6-bytesofthenextinstructionandstoresthemin the instruction queue and this process is known as instruction pre fetch. This process increases the speed of the processor.

- **SegmentRegisters:** Asegmentregistercontainstheaddressesofinstructionsanddatainmemorywhichareused by the processor to access memory locations. It points to the starting address of a memory segment currently being used.
  Thereare4segmentregistersin8086asgivenbelow:
  - **CodeSegmentRegister(CS):**Codesegment ofthememoryholdsinstructioncodesofa program.

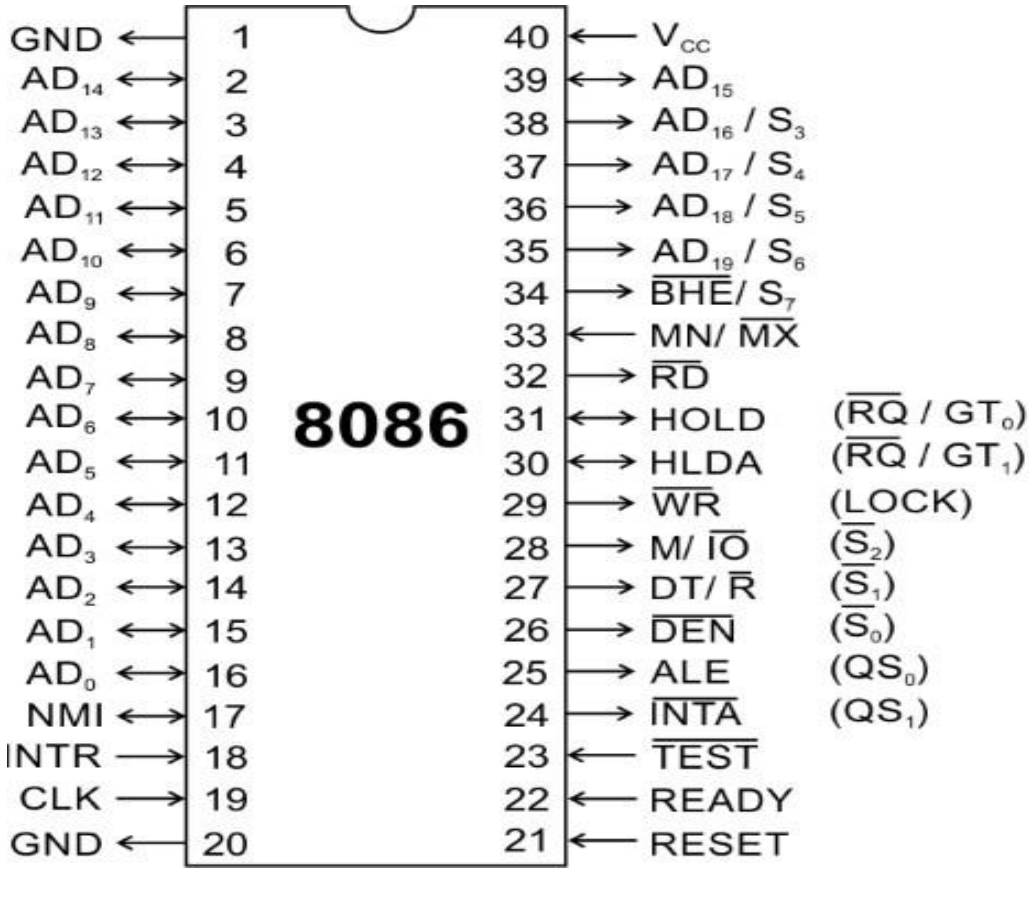
    - **DataSegmentRegister(DS):** Thedata,variablesandconstantsgiveninthe programareheldinthe data segment of the memory.
    - **StackSegmentRegister(SS):** Stacksegmentholdsaddressesanddataofsubroutines.Italsoholds the contents of registers and memory locations given in PUSH instruction.
    - **ExtraSegmentRegister(ES):**Extrasegmentholdsthedestinationaddresses ofsomedataof certain string instructions.
- **ALU:**Ithandlesallarithmeticandlogicaloperations.Suchasaddition,subtraction,multiplication,division, AND, OR, NOT operations.
- **Flag Register:** It isa 16-bit registerwhich exactly behaveslike a flip-flop, meansit changes states according to the resultstoredintheaccumulator.Ithas9 flagsandtheyaredividedinto2groups i.e.conditionalandcontrolflags.
- **ConditionalFlags:** Thisflagrepresentstheresultofthelastarithmeticorlogicalinstructionexecuted.Conditional flags are:
    - CarryFlag
    - AuxiliaryFlag
    - ParityFlag
    - ZeroFlag
    - SignFlag
    - OverflowFlag
- **ControlFlags:**Itcontrolstheoperationsoftheexecutionunit.Controlflagsare:
    - TrapFlag
    - InterruptFlag
    - DirectionFlag

5.2:SignalDescriptionofIntel8086.

Pindescription forIntel8086Microprocessor:

Intel**8086**isa16-bitHMOS**microprocessor**.Itisavailablein40**pin** DIPchip.Itusesa5VDCsupplyforitsoperation. The **8086** uses 20-line address bus.

The 8086 uses 20-line address bus. It has a 16-line data bus. The 20 lines of the address bus operate in multiplexed mode.The 16-loworderaddressbuslineshave been multiplexedwithdataand4 high-orderaddressbuslineshave been multiplexed with status signals.



AD0toAD15: TheselinesaremultiplexedAddress/data lines.WhenADlinesareusedtotransmitmemoryaddressA0- A15 is used and when data are transmitted over AD lines D-D15 is used.

A16-A19 Highorderaddresslines Thesearemultiplexedwithstatussignals.

A16/S3,A17/S4–A16andA17multiplexed withS3and S4respectivelyandS4andS3areusedtoselect thesegment outof the four segments.

A18/S5-A18multiplexedwithS5anditisusedasinterrupt flag.

A19/S6-A18multiplexedwithS6andS6isusedasbusmaster,whichhandlestheinternalbuscontrol.

BHE' / S7: BHE stands for Bus High Enable. It is an active low signal, i.e. it is active when it is low. It is used to indicate the transferofdataoverthehigherorderdatabus(D8toD15).BHE' decideswhetherthedatabuswillcarry16-bit dataor8-bit data.WhenBHE'isenabled(i.e.0),thenthebuswillcarry16-bit data,elseonly8-bit datathroughtheloworderdatabus lines. It is multiplexed with status pin S7.

RD': Itisareadsignalusedforreadoperation.Itisalsoanactivelowsignal.

READY: This is an acknowledgment signal from the slower I/O devicesor memory. When high, itindicatesthatthe deviceis ready to transfer data, else the microprocessor is in the wait state.

RESET: By using this pin, the program control returns to FFFF0$_H$. The signal is active High.

INTR: Thispinisusedtoreceiveaninterruptrequestsignal.Itisatypeofmaskable interrupt. **NMI:**

This is used for Non-Maskable Interrupt Request.

GND: Therearetwogroundpinsinthe8086,pin1andpin20.

VCC: Thepin40is forvoltage input.

TEST': Thisisalsoanactivelowsignal. Thispinisusedfor wait instructionwhenthe8086isconnectedwiththe8087 microprocessor.

CLK: Thispintellsabout theclock pulse.