LESSON PLAN (Winter-2024)			
Discipline: ETC	Semester: 3rd	Name of the Teaching Faculty: RAJAT KUMAR DUTTA	
Subject: DIGITAL ELECTRONICS	No of Days /per week class allotted:4	Semester From date: 01.07.2024 To 08.11.2024 No of Weeks:19	
Week	Class Day	Theory Topics	
1st		Unit-1: Basics of Digital Electronics (12)	
	1st	1.1 Number System-Binary, Octal, Conversion from one system to another number system.	
	2nd	Decimal, Hexadecimal - Conversion from one system to another number system.	
	3rd	1.2 Arithmetic Operation-Addition, Subtraction, Multiplication, Division,	
	4th	1's & 2's complement of Binary numbers& Subtraction using complements method	
2nd	1st	1.3 Digital Code & its application & distinguish between weighted & non-weigh Code, Binary codes, excess-3 and Gray codes.	
	2nd	1.4 Logic gates: AND,OR,NOT,NAND,-Symbol, Function, expression, truth table & timing diagram	
	3rd	NOR, Exclusive-OR, Exclusive-NORSymbol, Function, expression, truth table & timing diagram	
	4th	1.5 Universal Gates& its Realisation	
3rd 4th	1st	1.6 Boolean algebra, Boolean expressions, Demorgan's Theorems.	
	2nd	1.7 Represent Logic Expression: SOP & POS forms	
	3rd	1.8 Karnaugh map (3 & 4 Variables)&	
	4th	Minimization of logical expressions ,don't care conditions	
	1st	Unit-2: Combinational logic circuits (12)	
		2.1 Half adder, Full adder	
	2nd	Half Subtractor, Full Subtractor,	
	3rd	Serial Binary 4 bit adder.	
	4th	Parallel Binary 4 bit adder.	
5th	1st	2.2 Multiplexer (4:1),	
	2nd	De- multiplexer (1:4)	
	3rd	Decoder,	
	4th	Encoder	
6th	1st	Digital comparator (3 Bit)	
	2nd	Continue	
	3rd	2.3 Seven segment Decoder (Definition, relevance, gate level of circuit Logic circuit of above)	
	4th	Seven segment Decoder (truth table, Applications of above)	
	1st	Unit-3: Sequential logic Circuits (12) 3.1 Principle of flip-flops operation, its Types,	
	2nd	3.2 SR Flip Flop using NAND Latch (un clocked)	
7th	3rd	SR Flip Flop using NOR Latch (un clocked)	

I F	4th	3.3 Clocked SR Flip Flop-Symbol, logic Circuit, truth table and
	401	applications
	1st	D Flip Flop-Symbol, logic Circuit, truth table and applications
8th	2nd	JK FLIP FLOP-Symbol, logic Circuit, truth table and applications
l l	3rd	T Flip Flop-Symbol, logic Circuit, truth table and applications
	4th	JK Master Slave flip-flops-Symbol, logic Circuit, truth table and applications
	1st	Continue
	2nd	3.4 Concept of Racing and how it can be avoided.
9th	3rd	4.5 Concept of memories-RAM, ROM, static RAM, dynamic RAM,PS RAM
-	4th	4.6 Basic concept of PLD & applications
		Unit-4: Registers, Memories & PLD (8)
	1st	4.1 Shift Registers-Serial in Serial -out, Serial- in Parallel-out, Parallel in serial out and Parallel in parallel out
10th	2nd	4.2 Universal shift registers-Applications.
		4.3 Types of Counter & applications
	3rd	4.4 Binary counter,
	4th	Asynchronous ripple counter (UP & DOWN),
	1st	Decade counter.
	2nd	Synchronous counter,
11th	3rd	Ring Counter
	4th	Unit-5: A/D and D/A Converters (7) 5.1 Necessity of A/D converters
	1st	Necessity D/A converters.
12+h	2nd	5.2 D/A conversion using weighted resistors methods.
12th	3rd	Continue
	4th	5.2 D/A conversion using weighted resistors methods.
13th	1st	5.3 D/A conversion using R-2R ladder (Weighted resistors) network.
	2nd	Continue
	3rd	5.4 A/D conversion using counter method.
	4th	Continue
	1st	5.5 A/D conversion using Successive approximate method
14th	2nd	Continue
_	3rd	Unit-6: LOGIC FAMILIES (9)
-	4th	6.2 Characteristics of Digital ICs- Propagation Delay, fan-out, fan-in, Power Dissipation
45+1		
15th		
-	1st	Unit-6: LOGIC FAMILIES (9) 6.1 Varios logic families
16th	2nd	categories according to the IC fabrication process
-	3rd	6.2 Characteristics of Digital ICs- Propagation Delay,
	4th	fan-out, fan-in,
		Power Dissipation
	1st	Power Dissipation, Noise Margin,
1741	2nd	Power Supply requirement
17th	3rd	&Speed with Reference to logic families.
	4th	6.3 Features, circuit operation &various applications of TTL(NAND)
	1st	Features, circuit operation &various applications of CMOS (NAND)
	2nd	Continue
18th	3rd	Features, circuit operation &various applications of CMOS
		(NOR)
	4th	Continue

Rh. 2023

Signature of the Faculty