## **ACADEMIC LESSON PLAN OF WINTER 2023**

Discipline: ETC	Semester:3 <sup>RD</sup> Sem (G1)	Name of the Teaching Faculty: R. R. SETH and Smaranika Dalai
Subject: Digital Electronics Lab	No. of days/per week class allotted: 4p(4hr)/week	Semester From: 1 <sup>st</sup> Aug 2023 to 30 <sup>th</sup> Nov 2023 No. of Weeks: 17 weeks
Week	Class Day	Practical Topics
1 <sup>st</sup>	1 <sup>st</sup>	Introduction
	2 <sup>nd</sup>	Introduction
2 <sup>nd</sup>	1 <sup>st</sup>	EXP-1. Familiarization of Digital Trainer Kit & Digital ICs IE 7400, 7402, 7404, 7408, 7432 & 7486.(draw their pin diagram and features) (cont)
	2 <sup>nd</sup>	EXP-1 Familiarization of Digital Trainer Kit & Digital ICs IE 7400, 7402, 7404, 7408, 7432 & 7486.(draw their pin diagram ad features)
3 <sup>rd</sup>	1 <sup>st</sup>	EXP-2. Verify truth tables of AND, OR, NOT, NOR, NAND, XOR, XNOR gates using ICs& simplifications of Boolean gates (cont)
	2 <sup>nd</sup>	EXP-2. Verify truth tables of AND, OR, NOT, NOR, NAND, XOR, XNOR gates using ICs& simplifications of Boolean gates
4 <sup>th</sup>	1 <sup>st</sup>	EXP-3. Implement various gates by using universal properties of NAND & NOR gates verify and truth table tabulate data. (cont)
	2 <sup>nd</sup>	EXP-3. Implement various gates by using universal properties of NAND & NOR gates verify and truth table tabulate data.
5 <sup>th</sup>	1 <sup>st</sup>	EXP-4. Construct & verify operation of Half adder and Full adder using logic gates (cont)
	2 <sup>nd</sup>	EXP-4. Construct & verify operation of Half adder and Full adder using logic gates
6 <sup>th</sup>	1 st	EXP-5. Construct & verify operation of Half Subtractor and Full Subtractor using logic gates. (cont)
	2 <sup>nd</sup>	EXP-5. Construct & verify operation of Half Subtractor and Full Subtractor using logic gates.
7 <sup>th</sup>	1 <sup>st</sup>	EXP-6. Design &Implement a 4-bit Binary to Gray code converter (cont)
	2 <sup>nd.</sup>	EXP-6. Design &Implement a 4-bit Binary to Gray code converter.
8 <sup>th</sup>	1st	EXP-7. Design & Implement a Single bit/ two bit digital comparator circuit
		(cont)
	2 <sup>nd</sup>	EXP-7 Design & Implement a Single bit/ two bit digital comparator circuit
9 <sup>th</sup>	1 <sup>st</sup>	EXP-8. Design Multiplexer (4:1) and De-multiplexer (1:4). (cont)
	2 <sup>nd</sup>	EXP-8. Design Multiplexer (4:1) and De-multiplexer (1:4).
10 <sup>th</sup>	1 <sup>st</sup>	EXP-9. Study the operation of flip-flops (i)S-R flip flop (ii) J-K flip flop (iii) D flip
		flop (iv) T flip flop (cont)
	2 <sup>nd</sup>	EXP-9. Study the operation of flip-flops (i)S-R flip flop (ii) J-K flip flop (iii) D flip flop (iv) T flip flop
11 <sup>th</sup>	<b>1</b> st	EXP-10. Realize a 4-bit asynchronous UP/Down Counter. (cont)
	2 <sup>nd</sup>	EXP-10. Realize a 4-bit asynchronous UP/Down Counter.
12 <sup>th</sup>	1 <sup>st</sup>	EXP-11. Mini Project using Software: To collect data like pin configurations,
	'	display devices, Operational characteristics, applications and critical factors
		etc. on all digital ICs studied in theory and compile a project report throughout
		and submit at the end of the semester. To assemble and tests circuits using
		above digital ICs with test points e.g. Digital Clock / Frequency Counter /
		Running Glow Light upto 999/Solar cell &Opto coupler applications (cont)
	2 <sup>nd</sup>	EXP-11. Mini Project using Software: To collect data like pin configurations,
		display devices, Operational characteristics, applications and critical factors
		etc. on all digital ICs studied in theory and compile a project report throughout
		and submit at the end of the semester. To assemble and tests circuits using
		above digital ICs with test points e.g. Digital Clock / Frequency Counter /
		Running Glow Light upto 999/Solar cell &Opto coupler applications.
13 <sup>th</sup>	1 <sup>st</sup>	Lab practice
	2 <sup>nd</sup>	Lab practice
14 <sup>th</sup>	1 <sup>st</sup>	Lab practice
	2 <sup>nd</sup>	Lab practice
15 <sup>th</sup>	1 <sup>st</sup>	Lab practice
	2 <sup>nd</sup>	Lab practice
16 <sup>th</sup>	1 <sup>st</sup>	Sessional
	2 <sup>nd</sup>	Sessional
4 <b>7</b> th	1 <sup>st</sup>	Sessional
17 <sup>th</sup>	2 <sup>nd</sup>	Sessional
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