LESSON PLAN (Winter-2023)

Discipline: IT	Semester: 3rd	Name of the Teaching Faculty: P.BHAWANI
Subject: DIGITAL ELECTRONICS(TH-3)	No of Days /per week class allotted:4	Semester From date: 01.08.2023 To 30.11.2023 No of Weeks:15
Week	**Class Day**	**Theory Topics**
1st	1st	**Unit-1: Basics of Digital Electronics (12)** 1.1 Number System-Decimal,Binary, Conversion from one system to another number system.
	2nd	Octal, Hexadecimal - Conversion from one system to another number system.
	3rd	1.2 Arithmetic Operation-Addition, Subtraction, Multiplication, Division,
	4th	1's & 2's complement of Binary numbers& Subtraction using complements method
2nd	1st	1.3 Digital Code & its application & distinguish between weighted & non-weight Code, Binary codes, excess-3 and Gray codes.
	2nd	1.4 Logic gates: AND,OR,NOT,NAND,-Symbol, Function, expression, truth table & timing diagram
	3rd	NOR, Exclusive-OR, Exclusive-NOR-Symbol, Function, expression, truth table & timing diagram
	4th	1.5 Universal Gates& its Realisation
3rd	1st	1.6 Boolean algebra, Boolean expressions, Demorgan's Theorems.
	2nd	1.7 Represent Logic Expression: SOP & POS forms
	3rd	1.8 Karnaugh map (3 & 4 Variables)
	4th	Minimization of logical expressions ,don't care conditions
4th	1st	**Unit-2: Combinational logic circuits (12)** 2.1 Half adder, Full adder
	2nd	Half Subtractor, Full Subtractor,
	3rd	Serial Binary 4 bit adder.
	4th	Parallel Binary 4 bit adder.
5th	1st	2.2 Multiplexer (4:1),
	2nd	De- multiplexer (1:4)
	3rd	Decoder
	4th	Encoder
6th	1st	Digital comparator (2 Bit)
	2nd	Digital comparator (3 Bit)
	3rd	2.3 Seven segment Decoder (Definition, relevance, gate level of circuit Logic circuit of above)
	4th	2.3 Seven segment Decoder (Definition, relevance, gate level of circuit Logic circuit of above)
7th	1st	**Unit-3: Sequential logic Circuits (12)** 3.1 Principle of flip-flops operation, its Types
	2nd	3.2 SR Flip Flop using NAND Latch (un clocked)
	3rd	SR Flip Flop using NOR Latch (un clocked)
	4th	3.3 Clocked SR Flip Flop-Symbol, logic Circuit, truth table and applications
8th	1st	D Flip Flop-Symbol, logic Circuit, truth table and applications
	2nd	JK FLIP FLOP-Symbol, logic Circuit, truth table and applications
	3rd	T Flip Flop-Symbol, logic Circuit, truth table and applications
	4th	JK Master Slave flip-flops-Symbol, logic Circuit, truth table and applications

9th	1st	JK Master Slave flip-flops operation
	2nd	3.4 Concept of Racing and how it can be avoided.
	3rd	4.5 Concept of memories-RAM, ROM, static RAM, dynamic RAM,PS RAM
	4th	4.6 Basic concept of PLD & applications
10th	1st	**Unit-4: Registers, Memories & PLD (8)** 4.1 Shift Registers-Serial in Serial -out, Serial- in Parallel-out
	2nd	4.1 Parallel in serial out and Parallel in parallel out
	3rd	4.2 Universal shift registers-Applications. 4.3 Types of Counter & applications
	4th	4.4 Binary counter
11th	1st	Asynchronous ripple counter (UP & DOWN)
	2nd	Decade counter
	3rd	Synchronous counter, Ring Counter
	4th	4.5 Concept of memories-RAM, ROM, static RAM, dynamic RAM,PS RAM 4.6 Basic concept of PLD & applications
12th	1st	**Unit-5: A/D and D/A Converters (7)** 5.1 Necessity of A/D and D/A converters.
	2nd	5.2 D/A conversion using weighted resistors methods.
	3rd	5.3 D/A conversion using R-2R ladder (Weighted resistors)network.
	4th	5.4 A/D conversion using counter method.
13th	1st	5.5 A/D conversion using Successive approximate method
	2nd	Continue.
	3rd	Continue.
	4th	**Unit-6: LOGIC FAMILIES (9)** 6.1 Various logic families &categories according to the IC fabrication process
14th	1st	6.2 Characteristics of Digital ICs- Propagation Delay, fan-out, fan-in, Power Dissipationwith Reference to logic families.
	2nd	6.2 Characteristics of Digital ICs- Noise Margin ,Power Supply requirement &Speed with Reference to logic families.
	3rd	6.3 Features, circuit operation &various applications of TTL(NAND)
	4th	6.3 Features, circuit operation &various applications of TTL(NAND)
15th	1st	Features, circuit operation &various applications of CMOS (NAND)
	2nd	Features, circuit operation &various applications of CMOS (NOR)
	3rd	Continue.
	4th	Continue.

Signature of the Faculty