LESSON PLAN (WINTER-2021)

Discipline: ETC	Semester: 3rd	Name of the Teaching Faculty: KANAK PRAVA SWAIN
Subject: DIGITAL ELECTRONICS	No of Days /per week class allotted:4	Semester From date: 01.10.2021 To 08.01.2022 No of Weeks:15
Date	Class Day	Theory / Practical Topics
5.10.21	1st	Unit-1: Basics of Digital Electronics (12) 1.1 Number System-Binary, Octal, Conversion from one system to another number system.
7.10.21	2nd	Decimal, Hexadecimal - Conversion from one system to another number system.
9.10.21	3rd	1.2 Arithmetic Operation-Addition, Subtraction, Multiplication, Division,
9.10.21	4th	1's & 2's complement of Binary numbers& Subtraction using complements method
	1st	
	2nd 3rd	PUJA VACATION
	4th	
16.10.21	1st	1.3 Digital Code & its application & distinguish between weighted & non-weight Code, Binary codes, excess-3 and Gray codes.
21.10.21	2nd	1.4 Logic gates: AND,OR,NOT,NAND,-Symbol, Function, expression, truth table & timing diagram
21.10.21	3rd	NOR, Exclusive-OR, Exclusive-NORSymbol, Function, expression, truth table & timing diagram
23.10.21	4th	1.5 Universal Gates& its Realisation
26.10.21	1st	1.6 Boolean algebra, Boolean expressions, Demorgan's Theorems.
27.10.21	2nd	1.7 Represent Logic Expression: SOP & POS forms
28.10.21	3rd	1.8 Karnaugh map (3 & 4 Variables)&
28.10.21	4th	Minimization of logical expressions ,don't care conditions
30.10.21	1st	Unit-2: Combinational logic circuits (12) 2.1 Half adder, Full adder
2.11.21	2nd	Half Subtractor, Full Subtractor,
3.11.21	3rd	Serial Binary 4 bit adder.
3.11.21	4th	Parallel Binary 4 bit adder.
6.11.21	1st	2.2 Multiplexer (4:1),
9.11.21	2nd	De- multiplexer (1:4)
10.11.21	3rd	Decoder,
10.11.21	4th	Encoder
11.11.21	1st	Digital comparator (3 Bit)
13.11.21	2nd	Continue
16.11.21	3rd	2.3 Seven segment Decoder (Definition, relevance, gate level of circuit Logic circuit of above)

17.11.21	4th	Seven segment Decoder (truth table, Applications of above)
18.11.21	1st	Unit-3: Sequential logic Circuits (12) 3.1 Principle of flip-flops operation, its Types,
20.11.21	2nd	3.2 SR Flip Flop using NAND Latch (un clocked)
20.11.21	3rd	SR Flip Flop using NOR Latch (un clocked)
23.11.21	4th	3.3 Clocked SR Flip Flop-Symbol, logic Circuit, truth table and applications
24.11.21	1st	D Flip Flop-Symbol, logic Circuit, truth table and applications
25.11.21	2nd	JK FLIP FLOP-Symbol, logic Circuit, truth table and applications
27.11.21	3rd	T Flip Flop-Symbol, logic Circuit, truth table and applications
30.11.21	4th	JK Master Slave flip-flops-Symbol, logic Circuit, truth table and applications
30.11.21	1st	Continue
1.12.21	2nd	3.4 Concept of Racing and how it can be avoided.
2.12.21	3rd	4.5 Concept of memories-RAM, ROM, static RAM, dynamic RAM,PS RAM
4.12.21	4th	4.6 Basic concept of PLD & applications
7.12.21	1st	Unit-4: Registers, Memories & PLD (8) 4.1 Shift Registers-Serial in Serial -out, Serial- in Parallel-out, Parallel in serial out and Parallel in parallel out
8.12.21	2nd	4.2 Universal shift registers-Applications. 4.3 Types of Counter & applications
9.12.21	3rd	4.4 Binary counter,
11.12.21	4th	Asynchronous ripple counter (UP & DOWN),
14.12.21	1st	Decade counter. Synchronous counter,
15.12.21	2nd	Ring Counter
16.12.21	3rd	Unit-5: A/D and D/A Converters (7) 5.1 Necessity of A/D and D/A converters.
16.12.21	4th	5.2 D/A conversion using weighted resistors methods.
18.12.21	1st	5.3 D/A conversion using R-2R ladder (Weighted resistors)network.
21.12.21	2nd	5.4 A/D conversion using counter method.
22.12.21	3rd	5.5 A/D conversion using Successive approximate method
23.12.21	4th	Continue
28.12.21	1st	Unit-6: LOGIC FAMILIES (9)
29.12.21	2nd	6.1 Various logic families &
30.12.21	3rd	categories according to the IC fabrication process
4.1.22	4th	6.2 Characteristics of Digital ICs- Propagation Delay, fan-out, fan-in, Power Dissipation
4.1.22	1st	Noise Margin ,Power Supply requirement &Speed with Reference to logic families.
5.1.22	2nd	6.3 Features, circuit operation &various applications of TTL(NAND)
6.1.22	3rd	Features, circuit operation &various applications of CMOS (NAND)
8.1.22	4th	Features, circuit operation &various applications of CMOS (NOR)

Signature of the Faculty