LESSON PLAN (WINTER-2021)		
Discipline: ETC	**Semester:5th**	**Name of the Teaching Faculty: AMIT KUMAR NAYAK**
Subject: VLSI & Embedded System	**No of Days /per week class allotted: 4**	**Semester From date: 01.10.2021 To date: 08.01.2022** **No of Weeks:15**
Date	**Class Day**	**Theory / Practical Topics**
1.10.21	1st	**Unit-1: Introduction to VLSI & MOS Transistor(12)** 1.1 Historical perspective- Introduction
7.10.21	2nd	1.2 Classification of CMOS digital circuit types
8.10.21	3rd	1.3 Introduction to MOS Transistor& Basic operation of MOSFET.
9.10.21	4th	1.4 Structure and operation of MOSFET (n-MOS enhancement type) & COMS
	1st	**PUJA VACATION**
	2nd	
	3rd	
	4th	
9.10.21	1st	1.5 MOSFET V-I characteristics,
16.10.21	2nd	1.6 Working of MOSFET capacitances.
21.10.21	3rd	1.7 Modelling of MOS Transistors including Basic concept the SPICE level-1 models, the level-2 and level-3 model.
22.10.21	4th	1.8 Flow Circuit design procedures
23.10.21	1st	1.9 VLSI Design Flow & Y chart
23.10.21	2nd	1.10 Design Hierarchy
27.10.21	3rd	1.11 VLSI design styles-FPGA, Gate Array Design,
28.10.21	4th	Standard cells based, Full custom
29.10.21	1st	**Unit-2: Fabrication of MOSFET (10)** 2.1 Simplified process sequence for fabrication
30.10.21	2nd	2.2 Basic steps in Fabrication processes Flow
3.11.21	3rd	2.3 Fabrication process of nMOS Transistor
5.11.21	4th	2.4 CMOS n-well Fabrication Process Flow
5.11.21	1st	2.5 MOS Fabrication process by n-well on p-substrate
6.11.21	2nd	2.6 CMOS Fabrication process by P-well on n-substrate
10.11.21	3rd	2.7 Layout Design rules
11.11.21	4th	2.8 Stick Diagrams of CMOS inverter
12.11.21	1st	**Unit-3:MOS Inverter(09)** 3.1 Basic nMOS inverters,
13.11.21	2nd	3.2 Working of Resistive-load Inverter
17.11.21	3rd	3.3 Inverter with n-Type MOSFET Load – Enhancement Load,
17.11.21	4th	Depletion n-MOS inverter
18.11.21	1st	3.4 CMOS inverter – circuit operation and :

20.11.21	2nd	characteristics and interconnect effects Delay time definitions
24.11.21	3rd	3.5 CMOS Inventor design with delay constraints Two sample mask lay out for p-type substrate.
25.11.21	4th	**Unit-4: Static Combinational, Sequential, Dynamics logic circuits & Memories(15)** 4.1 Define Static Combinational logic ,working of Static CMOS logic circuits (Two-input NAND Gate)
25.11.21	1st	4.2 CMOS logic circuits (NAND2 Gate)
26.11.21	2nd	4.3 CMOS Transmission Gates(Pass gate)
27.11.21	3rd	4.4 Complex Logic Circuits - Basics
1.12.21	4th	4.5 Classification of Logic circuits based on their temporal behaviour
2.12.21	1st	**Continue**
3.12.21	2nd	4.6 SR Flip latch Circuit,
4.12.21	3rd	**Continue**
4.12.21	4th	4.7 Clocked SR latch only.
8.12.21	1st	**Continue**
9.12.21	2nd	4.8 CMOS D latch.
10.12.21	3rd	4.9 Basic principles of Dynamic Pass Transistor Circuits
11.12.21	4th	4.10 Dynamic RAM,
15.12.21	1st	SRAM,
15.12.21	2nd	4.11 Flash memory
16.12.21	3rd	**Unit-5: System Design method & synthesis (04)** 5.1 Design Language (SPL & HDL)& HDL & EDA tools & VHDL and packages Xlinx
17.12.21	4th	5.2 Design strategies & concept of FPGA with standard cell based design
18.12.21	1st	5.3 VHDL for design synthesis using CPLD or FPGA
22.12.21	2nd	5.4 Raspberry Pi - Basic idea
23.12.21	3rd	**Unit-6: Introduction to Embedded Systems(10)** 6.1 Embedded Systems Overview,list of embedded systems,characteristics ,
24.12.21	4th	example – A Digital Camera
29.12.21	1st	6.2 Embedded Systems Technologies--Technology – Definition. -Technology for Embedded Systems
30.12.21	2nd	Processor Technology, IC Technology
30.12.21	3rd	6.3 Design Technology-Processor Technology,General Purpose Processors – Software,
31.12.21	4th	Basic Architecture of Single Purpose Processors – Hardware
5.1.22	1st	6.4 Application – Specific Processors,Microcontrollers,Digital Signal Processors(DSP)
6.1.22	2nd	6.5 IC Technology- Full Custom / VLSI,Semi-Custom ASIC
7.1.22	3rd	(Gate Array & Standard Cell), PLD (Programmable Logic Device)
8.1.22	4th	6.6 Basic idea of Arduino micro controller

Signature of the Faculty