**LESSON PLAN (Winter-2022)**

| Discipline: IT | Semester: 3rd | Name of the Teaching Faculty: P Bhawani |
|---|---|---|
| Subject: DIGITAL ELECTRONICS | No of Days /per week class allotted:4 | Semester From date:    15.09.2022  To   22.12.2022<br>No of Weeks:14 |

| Week | Class Day | Theory  Topics |
|---|---|---|
| 1st | 1st | **Unit-1: Basics of Digital Electronics (12**)<br>1.1 Number System-Binary, Octal, Conversion from one system to another number system. |
| | 2nd | Decimal, Hexadecimal - Conversion from one system to another number system. |
| | 3rd | 1.2 Arithmetic Operation-Addition, Subtraction, Multiplication, Division, |
| | 4th | 1's & 2's complement of Binary numbers& Subtraction using complements method |
| 2nd | 1st | 1.3 Digital Code & its application & distinguish between weighted & non-weight Code, Binary codes, excess-3 and Gray codes. |
| | 2nd | 1.4 Logic gates: AND,OR,NOT,NAND,-Symbol, Function, expression, truth table & timing diagram |
| | 3rd | NOR, Exclusive-OR, Exclusive-NOR--Symbol, Function, expression, truth table & timing diagram |
| | 4th | 1.5 Universal Gates& its Realisation |
| 3rd | | **PUJA VACATION** |
| 4th | 1st | 1.6 Boolean algebra, Boolean expressions, Demorgan's Theorems. |
| | 2nd | 1.7 Represent Logic Expression: SOP & POS forms |
| | 3rd | 1.8 Karnaugh map (3 & 4 Variables)& |
| | 4th | Minimization of logical expressions ,don't care conditions |
| 5th | 1st | **Unit-2: Combinational logic circuits (12)**<br>2.1 Half adder, Full adder |
| | 2nd | Half Subtractor, Full Subtractor, |
| | 3rd | Serial  Binary 4 bit adder. |
| | 4th | Parallel Binary 4 bit adder. |
| 6th | 1st | 2.2 Multiplexer (4:1), |
| | 2nd | De- multiplexer (1:4) |
| | 3rd | Decoder, |
| | 4th | Encoder |
| 7th | 1st | Digital comparator (3 Bit) |
| | 2nd | Continue… |
| | 3rd | 2.3 Seven segment Decoder (Definition, relevance, gate level of circuit Logic circuit of above) |
| | 4th | Seven segment Decoder (truth table, Applications of above) |
| 8th | 1st | **Unit-3: Sequential logic Circuits (12)**<br>3.1 Principle of flip-flops operation, its Types, |
| | 2nd | 3.2 SR Flip Flop using NAND  Latch (un clocked) |
| | 3rd | SR Flip Flop using NOR Latch (un clocked) |
| | 4th | 3.3 Clocked SR Flip Flop-Symbol, logic Circuit, truth table and applications |
| | 1st | D Flip Flop-Symbol, logic Circuit, truth table and applications |

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| 9th | 2nd | JK FLIP FLOP-Symbol, logic Circuit, truth table and applications |
| | 3rd | T Flip Flop-Symbol, logic Circuit, truth table and applications |
| | 4th | JK Master Slave flip-flops-Symbol, logic Circuit, truth table and applications |
| 10th | 1st | Continue… |
| | 2nd | 3.4 Concept of Racing and how it can be avoided. |
| | 3rd | 4.5 Concept of memories-RAM, ROM, static RAM, dynamic RAM,PS RAM |
| | 4th | 4.6 Basic concept of PLD & applications |
| 11th | 1st | **Unit-4: Registers, Memories & PLD (8)**<br>4.1 Shift Registers-Serial in Serial -out, Serial- in Parallel-out, Parallel in serial out and Parallel in parallel out |
| | 2nd | 4.2 Universal shift registers-Applications.<br>4.3 Types of Counter & applications |
| | 3rd | 4.4 Binary counter, |
| | 4th | Asynchronous ripple counter (UP & DOWN), |
| 12th | 1st | Decade counter. Synchronous counter, |
| | 2nd | Ring Counter |
| | 3rd | **Unit-5: A/D and D/A Converters (7)**<br>5.1 Necessity of A/D and D/A converters. |
| | 4th | 5.2 D/A conversion using weighted resistors methods. |
| 13th | 1st | 5.3 D/A conversion using R-2R ladder (Weighted resistors)network. |
| | 2nd | 5.4 A/D conversion using counter method. |
| | 3rd | 5.5 A/D conversion using Successive approximate method |
| | 4th | Continue….. |
| 14th | 1st | **Unit-6: LOGIC FAMILIES (9)** |
| | 2nd | 6.1 Various logic families & |
| | 3rd | categories according to the IC fabrication process |
| | 4th | 6.2 Characteristics of Digital ICs- Propagation Delay, fan-out, fan-in, Power Dissipation |
| 15th | 1st | Noise Margin ,Power Supply requirement &Speed with Reference to logic families. |
| | 2nd | 6.3 Features, circuit operation &various applications of TTL(NAND) |
| | 3rd | Features, circuit operation &various applications of  CMOS (NAND ) |
| | 4th | Features, circuit operation &various applications of CMOS ( NOR) |

15/09/2022

Signature of the Faculty