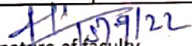


## LESSON PLAN WINTER 2022

Department: Information Technology	Semester : 3 <sup>rd</sup>	Name of the Teaching faculty: Pranati Pattnaik	
Subject :- Computer System and Architecture	No. of Days/ week class allotted : 04/week	Semester from date: 15/09/2022 to 22/12/2022	No. of Weeks :15
Week	Class Day	Topics	Remarks
1 <sup>st</sup> Week: (15 th Sept-17th Sept)	1 <sup>st</sup>	Basic Structure of computer hardware	
	2 <sup>nd</sup>	Functional Units	
2 <sup>nd</sup> Week: (19 th Sept - 24 th Sept)	1 <sup>st</sup>	Computer components	
	2 <sup>nd</sup>	Performance measures	
	3 <sup>rd</sup>	Memory addressing & Operations	
	4 <sup>th</sup>	Instructions & instruction Sequencing Fundamentals to instructions	
3 <sup>rd</sup> Week: (26 th Sept-1st Oct)	1 <sup>st</sup>	Operands, Op Codes	
	2 <sup>nd</sup>	Instruction Formats	
	3 <sup>rd</sup>	Addressing Modes	
	4 <sup>th</sup>	Register Files	
4 <sup>th</sup> week	<b>vacation</b>	<b>Puja Vacation</b>	
5 <sup>th</sup> Week: (10 th Oct- 15 th Oct)	1 <sup>st</sup>	Decode, Execution, Complete instruction execution & Fetch	
	2 <sup>nd</sup>	Hardware control, Micro program control, Micro program control	
	3 <sup>rd</sup>	REVISION	
	4 <sup>th</sup>	Memory System	
6 <sup>th</sup> Week: (17 th Oct- 22 nd Oct)	1 <sup>st</sup>	Memory characteristics	
	2 <sup>nd</sup>	Memory hierarchy	
	3 <sup>rd</sup>	REVISION	
	4 <sup>th</sup>	RAM and ROM organization	
7 <sup>th</sup> Week: (25 th Oct- 31 st Oct)	1 <sup>st</sup>	Interleaved Memory	
	2 <sup>nd</sup>	Cache memory	
	3 <sup>rd</sup>	Virtual memory	
	4 <sup>th</sup>	REVISION	
8 <sup>th</sup> Week: (1st Nov- 5th Nov)	1 <sup>st</sup>	Input - Output Interface	
	2 <sup>nd</sup>	Modes of Data transfer	
	3 <sup>rd</sup>	Programmed I/O Transfer	
	4 <sup>th</sup>	Interrupt driven I/O	
9 <sup>th</sup> Week: (7 th Nov -12 th Nov)	1 <sup>st</sup>	DMA	
	2 <sup>nd</sup>	REVISION	
	3 <sup>rd</sup>	I/O Processor	
	4 <sup>th</sup>	Bus and System Bus	
10 <sup>th</sup> Week: (14 th Nov -19 th Nov)	1 <sup>st</sup>	Data, Address, Control	
	2 <sup>nd</sup>	Bus Structure	
	3 <sup>rd</sup>	Basic Parameters of Bus design	
	4 <sup>th</sup>	SCSI	
11 <sup>th</sup> Week: (21st Nov - 26 th Nov)	1 <sup>st</sup>	USB	
	2 <sup>nd</sup>	Parallel Processing	
	3 <sup>rd</sup>	REVISION	
	4 <sup>th</sup>	Linear Pipeline	
12 <sup>th</sup> Week: (28 th Nov -3 rd Dec)	1 <sup>st</sup>	Linear Pipeline	
	2 <sup>nd</sup>	Multiprocessor	
	3 <sup>rd</sup>	REVISION/TEST	
13 <sup>th</sup> Week: (5 th Dec -10 th Dec)	1 <sup>st</sup>	Flynn's Classification	
	2 <sup>nd</sup>	Single Instruction Single Data Stream	
	3 <sup>rd</sup>	Single Instruction Single Data Stream	
14 <sup>th</sup> Week: ( 12 th Dec- 17th Dec)	1 <sup>st</sup>	Single Instruction Multiple Data Stream	
	2 <sup>nd</sup>	Single Instruction Multiple Data Stream	
	3 <sup>rd</sup>	Multiple Instruction Multiple Data Stream	
	4 <sup>th</sup>	REVISION/TEST	
15 <sup>th</sup> Week: (19 th Dec- 22nd Dec)	1 <sup>st</sup>	Multiple Instruction Single Data Stream	
	2 <sup>nd</sup>	Multiple Instruction Single Data Stream	
	3 <sup>rd</sup>	Multiple Instruction Multiple Data Stream	
	4 <sup>th</sup>	REVISION/TEST	

  
 Signature of faculty